MULLARD LIMITED
Mullard House
Torrington Place
London, W.C.1

CONTENTS

Thermal Resistance of Semiconductor Devices under Steady-state Conditions 127–140

Transistorised SCR Firing Circuits 141–157

Switch-off Circuits for SCRs Operating on d.c. 158–161

Precise Phase Angle Control of SCRs 162–168

VOL. 7 No. 65 JUNE 1963

Mullard Technical Communications

VOLUME 7 NUMBER 65 June 1963

Mullard Technical Communications

VOLUME 7 NUMBER 65 June 1963

Contents

Thermal Resistance of Semiconductor Devices under Steady-state Conditions *P. Coleby* 127

Transistorised SCR Firing Circuits *T. J. Jarratt* 141

Switch-off Circuits for SCRs Operating on d.c. *R. A. Payne and E. S. Reeves* 158

Precise Phase Angle Control of SCRs *R. A. Payne* 162

Mullard Technical Communications contains information on the performance or application of Mullard products such as electronic valves and tubes, semiconductor devices and electrical and magnetic components. It is issued free-of-charge to equipment designers, research organisations, reference libraries and educational establishments. Bona fide applications to be added to the circulation list should be made under an official letter head to the Technical Information Department. Overseas enquiries should be addressed to the local Mullard agent, or to Mullard Overseas Ltd. at Mullard House.

Abstracts or references to an article should mention both the source, *Mullard Technical Communications*, and the authors. Requests for re-publication or translation should be made to the Editor in writing.

The issue of the information contained in this publication does not imply any authority or licence for the utilisation of any patented feature.

Mullard is the trade mark of Mullard Limited and is registered in most of the principal countries of the world.

Editor: F. A. Sowan

Assistant Editors: E. G. Evans R. Barrie

Published by
Technical Information Department
Mullard Limited, Mullard House, Torrington Place, London, W.C.1
LANgham 6633

© Mullard Limited, 1963

Made and Printed in England by
WIGHTMAN AND COMPANY LIMITED, 1/3 BRIXTON ROAD, LONDON, S.W.9

EDITORIAL

Some people might argue that too much information can be published about an electronic device, possibly leading to confusion and difficulty for the user. It seems to us that two types of information are called for. First of all, we should give simple instructions as to how to use the device in some sort of stacked assembly – treating it as a black box with input and output terminals. But the more appreciative engineer will either need more information to assess operation under unusual conditions, or he will wish to learn all about the finer points of stressing and operation – not only to satisfy his own curiosity, but to provide a firm basis for future circuit design.

The present issue of *Mullard Technical Communications* is largely concerned with silicon controlled rectifiers and their operation. In the field of rectification (whether SCRs or diode rectifiers are used), some engineers will merely wish to achieve a finished equipment with a certain specified performance; and they will wish to expend the minimum of effort on what may seem a secondary portion of the equipment. For them, tables of design centre values for operation from standard supply mains are provided in data sheets. For those engineers with a wider interest, however, we publish detailed applications articles, with circuit design procedures and illustrative examples.

In this issue are three articles on SCR operation, and one on the design of heatsinks for semiconductor devices. The SCR articles are part of a series on many aspects of this relatively new device.

The problems of transistorised firing circuits for SCRs are many and various. Some of the basic circuits are surveyed in the article on page 141, and illustrative practical circuits are given in the appendix on page 150. In the design of these circuits, several types of spread have to be taken into account: the spread of the gate characteristics of the SCR, the resistor and capacitor tolerances, and mains voltage fluctuations. These spreads bring design problems that we hope to discuss more fully in later articles which will take individual types of firing circuit and examine them in detail.

Operation of SCRs from d.c., either to replace a resistance 'drum controller' or to generate a.c. from d.c., is of great interest. Until the SCR with switch-off characteristics on the gate becomes an economic proposition, interest is centred on the size of capacitor necessary to switch off an SCR on its anode, and on the recovery time of the device itself. The article on page 158 is, again, of an introductory nature.

The third SCR article in this issue, on page 162, covers a fully-toleranced circuit for precision firing angle control. The remaining article, which opens the issue, is the latest contribution to our published work on the thermal resistance of semiconductor devices. It brings earlier articles up to date, and describes practical techniques for the determination of theta.

In the Mullard application laboratories we continue with the many aspects of application work on electronic devices. We believe that this work, once thoroughly done on any particular circuit, and with full tolerancing of all components, should be published for all users of these devices, thus saving the time and expense of repeating the same work over and over again in customers' premises.

MULLARD TECHNICAL COMMUNICATIONS
Vol. 7, No. 64

Stereophonic Tape Recorder

We regret that there are several errors in the circuit diagram of the 3W tape amplifier (Fig. 1, page 111).

The lower terminal of the radio input should be connected to chassis, and not left floating. The connection from the top of S_{B1} should be taken to the right-hand end of R_{12}, and not to the left. The value of C_8 should be 180pF, not 180μF. The junction of R_{26} and C_{19} should be taken to the record-playback line (from C_{22} to S_{A3}) and not to chassis. The line from the top of L_3 should cross the chassis line without connection. Transformer T_1 should be shown with laminations, not with a dust core.

Low-voltage Pocket Portable Radio Receiver

The base of Tr_7 should be connected to the collector of Tr_5, not to the emitter. The loudspeaker impedance is 10Ω.

Thermal Resistance of Semiconductor Devices under Steady-state Conditions

P. Coleby
Mullard Semiconductor Measurement and Application Laboratory

The junctions of semiconductor diodes or transistors must not exceed their maximum temperature ratings. The temperature attained is determined mainly by the electrical dissipation at the junctions and by the ability of the device to transfer heat to its surface, to any auxiliary dissipators (flags, fins, or heatsinks), and thence to ambient. Thus the thermal resistance of all the conductive, convective, and radiative heat-paths must be known.

The calculation of thermal resistances and power ratings, and the design of dissipators, are discussed; and an apparatus is described which facilitates monitoring of the junction temperature by observation of a temperature-sensitive parameter (normally the forward voltage) of the device. A simple and reliable null-reading technique is used.

GENERAL CONCEPTS

For safe and efficient operation of semiconductor devices, it is essential that the maximum rated junction temperature is not exceeded. Therefore thermal resistance—the dependence of junction temperature on device dissipation—is one of the parameters always given in published data, and its measurement is of considerable importance.

Definitions

The thermal resistance of semiconductor devices is defined (Ref. 1) as follows:

> '*Thermal Resistance, Effective (of a Semiconductor Device):*
>
> The effective temperature rise per unit power dissipation of a designated *junction* above the temperature of a stated external reference point under conditions of thermal equilibrium.'

Under steady-state conditions, the thermal resistance of any thermal conductor is the ratio of the temperature drop across the conductor to the heat transfer rate through it.

When a continuous power is dissipated in a semiconductor device, the heat generated will cause the junction temperature to rise until the temperature difference between junction and ambient (that is, the final cooling medium) is such that a stable thermal state exists. In this state, the heat transference from the device is equal to the heat generated in the device.

Although the heat is transferred by conduction, convection, and radiation, in general we are concerned with the overall heat transference from the junction to the surroundings. As the expression for current transfer, $I = E/R$, is comparable with that for heat transfer, we may use an electrical analogue in which current represents heat flow, voltage represents temperature difference, and resistance represents the opposition to the flow of heat energy—that is, the thermal resistance.

Units and Symbols

The unit of heat transfer is joules per second (watts). The unit of thermal resistance may be either degC/W or degC/mW, the choice of unit depending on the power-handling capacity of the device.

The British Standards symbol for thermal resistance (Ref. 2) is theta (θ), used with suitable subscripts. Other symbols have been used, but they are not recommended.

The symbol θ with no subscript is generally used to denote the total or overall thermal resistance. If a single subscript is used to denote a particular component of the overall thermal resistance, either an equivalent thermal resistance circuit or a clear definition should be given. However, in many cases the use of two subscripts may be sufficient to make the relevant thermal resistance clear at sight.

Typical subscripts are:

j = junction   a = ambient
c = case (or e = envelope)   m or mb = mounting base
i = infinite heatsink   h or hs = heatsink

Thermal Analogue

It is generally assumed that the heat transfer is by one main path, from the junction to the envelope of the device and then from the envelope to the ambient. There is an alternative path via the lead-out wires, but in most instances the simple approximation is still valid, as this is a minor heat path.

With power transistors, where the crystal is directly connected to the header, typical internal thermal resistance values of from 7·5degC/W to < 1degC/W are obtained. But when the envelope of the device is the sole heat dissipator, the external thermal resistance is so large in proportion that the overall value is approximately equal to the external value. For example, for the OC28 in

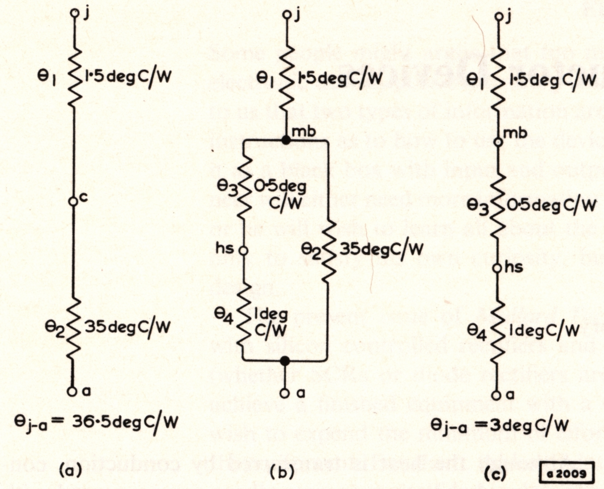


Fig. 1—Equivalent circuits for high-power transistor

TO-3 envelope,

$$\theta_{c-a} = 35\text{degC/W} \quad \text{and} \quad \theta_{j-c} = 1{\cdot}5\text{degC/W}.$$

The corresponding equivalent circuit is shown in Fig. 1a.

Beyond a limit of about 300 to 400mW, it becomes impracticable to increase the size of the base and the thickness of the leads to reduce the external thermal resistance to a value comparable to the internal thermal resistance; therefore power devices are specifically designed for mounting on a heatsink. The effect of a heatsink or dissipator is to increase the effective heat-dissipation area. On the equivalent circuit, the effect is to produce an alternative low thermal resistance path to the heat flow from the case to the ambient, shown as $\theta_3+\theta_4$ in Fig. 1b, where θ_3 is the thermal resistance between the mounting base and heatsink by conduction (typically 0·2 to 3degC/W), and θ_4 is the thermal resistance from heatsink to ambient by radiation and convection (typically 1 to 10degC/W).

In order to utilise the full power-handling capacity of a device as indicated by θ_{j-c}, there must be no temperature rise between case and ambient. Such a condition occurs only when the external thermal resistance (θ_{c-a}) is zero; that is, when the device is mounted on a hypothetical infinite heatsink. The concept of an infinite heatsink is used when defining the internal thermal resistance between junction and case; in practice it can never be realised.

The greater the ratio of θ_{j-c} to θ_{c-a}, the closer is the approximation to an infinite heatsink; and the power-handling capacity of the device approaches the limit defined by θ_{j-c}. With power devices, where θ_{j-c} is low, very large heatsinks are required to obtain low enough values of θ_{c-a} to utilise the full power-handling capacity. At lower dissipation levels, smaller heatsinks (1 to 10degC/W) may be safely tolerated with a consequent saving of space, unless the temperature rise is to be restricted to improve the stability of temperature-sensitive parameters.

When a heatsink is used, the radiation and convection from the case are generally small enough to be ignored (that is, $\theta_2 \gg \theta_3+\theta_4$), and the circuit simplifies to that shown in Fig. 1c.

Heatsinks

Any form of plate, flag, or cylinder that increases the effective heat-dissipating area of a device, and hence the radiation and convection losses, will reduce the external component of thermal resistance. Generally, when the published data sheet of a low-power device gives two values of thermal resistance—the overall value (θ_{j-a}) and the internal value (θ_{j-c})—a comparison of the two figures will show that the external value constitutes a significant proportion of the whole. In such instances a considerable improvement in power-handling capacity may be obtained by the use of a dissipator.

For metal envelopes of the TO-5, TO-9, and other types, the external value of thermal resistance is considerable, say 210degC/W. Commercial forms of finned cylinder or flag dissipator, for use in free air, have a typical value of 70degC/W. The use of such a dissipator can reduce the value θ_{c-a} to 52degC/W, as shown in Fig. 2. If the internal thermal resistance of the device is comparatively low (< 100degC/W) even $\theta_{c-a} = 50$degC/W is still significant, and a considerable increase in power-handling capacity may be obtained with a larger heatsink.

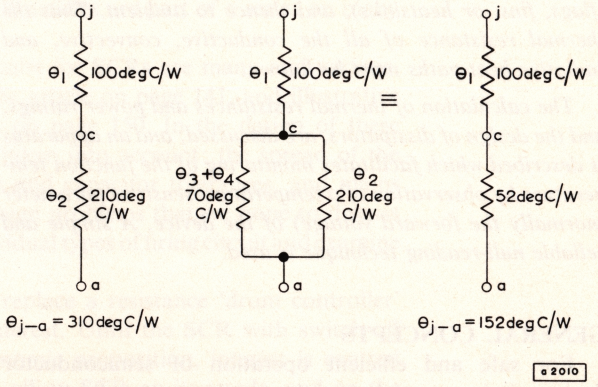


Fig. 2—Equivalent circuits for low-power transistor

Both flag and cylindrical finned types generally rely on a tight friction fit between the metal envelope and the heatsink for good conductive heat transfer. Some forms of flag or finned cylinder are designed for mounting, if required, on to a larger heatsink. Care should be taken to ensure a good thermal connection to the main heatsink, as a value of contact thermal resistance of say 10degC/W will largely nullify the advantage offered by the larger surface area.

Considerable work has been done in the field of heatsinks for power devices, and commercial forms of heatsink are available in the range 1·5degC/W to 3degC/W. These heatsinks are generally of the finned variety, where the necessarily large surface area is obtained in a comparatively limited space. Where an excessively large heatsink is to be avoided, the following general points should be noted.

Heat is dissipated from the heatsink by convection and radiation. In both cases the surface area, although it is important, is not the only factor that must be considered. The temperature difference, the conductivity, thickness, and emissivity of the material, the shape and orientation of the heatsink, and the type of convection, all play their part (Refs. 3, 4).

To avoid an excessive temperature gradient in the heatsink itself, a high-conductivity material should be used. Copper and aluminium, with conductivities of 3·8 and 2·3W/cm degC respectively, are the most usual materials. For the same surface conditions an aluminium heatsink should be 3·8/2·3 times thicker than the corresponding copper heatsink, to obtain the same value of thermal resistance.

Radiation losses may be increased by improving the surface. Best results are obtained with matt black finishes, typical emissivities being of the order of 0·9.

For free air conditions, vertical mounting gives improved convective losses. As a rough guide, 25% to 30% more area is required if the plate is horizontally mounted. When air is free to move over both faces, the total surface area is effective. The use of a chassis as a heatsink, where the air flow is restricted to one side, gives a reduction of the effective area by approximately a half.

For calculation of losses, the area considered is the total area. However, with a plane heatsink (for example, 10in × 10in) the size of the heatsink may be defined either by the total area (200in^2) or by the area of one face (100in^2).

If a plane, vertical, blackened copper heatsink ⅛in thick, in free air, is taken as a standard, the following table gives a rough pessimistic guide to the total area required.

θ(degC/W)	10	5	2	1
Total area (in^2)	10	40	100	200

At high ambient temperatures, in restricted spaces, or for values of $\theta \leqslant 1$degC/W, forced air convective cooling is often used to reduce the effective thermal resistance of a heatsink.

The most practical way of obtaining a nearly 'infinite' heatsink is by liquid convection cooling. With transformer oil as coolant, a typical figure of 10degC/W for each square inch of heatsink area may be obtained.

In all critical cases, the calculated value should only be taken as a guide, and the actual value of thermal resistance should be practically verified. This is generally done by monitoring the mounting base or stud temperature with a thermocouple.

Thermal Resistance Mounting Base to Heatsink

A thermal resistance θ_3 is shown in Fig. 1, between the mounting base and the heatsink of the power transistor. There are two reasons for this:

(i) When a single heatsink is used for several devices, some form of electrical insulation is often necessary. Unfortunately, good electrical insulators are generally poor thermal conductors, so the insertion of an insulating medium may considerably increase the thermal resistance between mounting base and heatsink.

The most common method of insulating the devices is by means of a mica or Teflon washer. Mica has a lower electrical resistance and dielectric strength than Teflon, but a considerably lower thermal resistivity. Washer thicknesses vary from 1 to 5 thousandths of an inch, being governed by both mechanical and electrical considerations.

An alternative method is to deposit a thin insulating layer on either the device or the heatsink by means of anodising or similar techniques. It is desirable to check electrically that no short-circuit exists.

(ii) When trying to simulate an infinite heatsink or to obtain a very low external θ, the thermal resistance of the insulation (0·2degC/W to 3degC/W) may be too great to be tolerated. Individual heatsinks requiring no insulation are then necessary. Even without an insulating layer, some thermal resistance exists because of the presence of a thin layer of air between the two surfaces. This is the contact or interface thermal resistance.

For low contact resistance, the following conditions are required:

(i) Sufficient pressure. Generally, a specified torque is given for stud-mounted devices. For example, for the following Unified Screw Threads:

Thread	Torque (lb-in)
No. 10—32 UNF	15
¼—28 UNF	30
½—20 UNF	150

(ii) A plane surface to the heatsink. This should be machined or punched and free from burrs.

(iii) A plane mounting base on the device. This is the manufacturer's responsibility. Tolerances of 0° to 0°20′ and 0° to 0°30′ are typical.

A common method of reducing the interface thermal resistance produced by the air layer is to substitute an alternative medium with a lower thermal resistance, such as a thin film of oil or grease. Silicon compounds, which have a higher conductivity and are non-corrosive to metals and impervious to moisture, are often used. A reduction in the interface thermal resistance of from 20% to 40% is often possible by this means.

When two poor mating surfaces give a high interface thermal resistance, an improvement may be achieved by using a thin lead or solder washer to 'pick up' any irregularities. The thickness of the washer may be several thousandths of an inch.

Relative Importance of Internal Thermal Resistance in Determining Power-handling Capacity

From the I.R.E. definition, the general formula for thermal resistance is:

$$\theta_{s-r} = (t_s - t_r)/P_s \qquad \ldots(1)$$

where t = temperature in °C, P = power, s and r = source and reference respectively. Therefore by simple transposition of the general formula

$$P_s = \frac{t_s - t_r}{\theta_{s-r}}\,. \qquad \ldots(1a)$$

A high power-handling capacity may be obtained by the use of a device having a low internal thermal resistance mounted on a large heatsink, as previously discussed. However, there are two other possible means of obtaining a high value of maximum dissipation, both of which increase the numerator of the right-hand side of Eq(1a).

(i) *Low reference temperature* (t_r)

If the ambient temperature (t_a) is taken as reference, the permissible temperature rise (t_s-t_r) may be increased, and consequently P_s increased, by reducing t_a. In equipment design this would entail adequate ventilation, possibly forced convection cooling, and, where possible, isolation of the device from major heat sources.

(ii) *High source temperature* (t_s)

The alternative method is to increase t_s; that is, to select a device with a high $t_j$max. The permitted value of $t_j$max for silicon devices is from 150°C to 200°C, whilst for germanium devices it is only 75°C to 100°C. Therefore, for given values of θ_{s-r} and t_r, the maximum dissipation for a silicon device is far greater than for a germanium device, the more so for a device whose $t_j$max is 200°C compared to another whose $t_j$max is 150°C.

Significance of θ_{j-c}

Consider two devices, A with θ_{j-c} = 1degC/W, and B with θ_{j-c} = 2degC/W. Only when mounted on infinite heatsinks, all other things being equal, will device A have double the power rating of device B. In those instances where a low external thermal resistance is unnecessary, the internal value may give very little indication of the relative power-handling capacity of the devices.

For example, device A, with θ_{j-c} = 1degC/W, mounted on a heatsink such that θ_{c-a} = 5degC/W (that is, with an overall thermal resistance of 6degC/W) will, all other things being equal, have a smaller power-handling capacity than device B mounted on a heatsink such that θ_{c-a} = 2degC/W (that is, with an overall thermal resistance of 4degC/W).

Device B, even with the same value of θ_{c-a} (2degC/W), provided that it has a higher permissible $T_j$max, may have a greater maximum power-handling capacity than device A.

Thus, let the reference temperature be 60°C. If $t_j$max of device A is 75°C and $t_j$max of device B is 90°C, then from Eq(1a)

$$\text{for device A:}\quad P_s = \frac{75-60}{(1+2)} = 5\text{W}.$$

$$\text{and for device B:}\quad P_s = \frac{90-60}{(2+2)} = 7{\cdot}5\text{W}.$$

THERMAL RESISTANCE MEASUREMENT

From the general expression for the thermal resistance between source and reference

$$\theta_{s-r} = \frac{t_s - t_r}{P_s}$$

it may be seen that two sets of measurements are necessary to determine the thermal resistance.

(i) Temperature measurements to give the temperature difference between source and reference.

(ii) Voltage and current measurements to give the source dissipation.

Temperature Measurements

External measurements of the reference temperature are made by conventional means. However, because of the inaccessibility of the junction, it is necessary to determine the junction temperature in terms of some internal temperature-sensitive parameter.

Initially, when germanium devices predominated, the parameter most commonly used was the reverse current I_{CBO}. For a general-purpose measuring equipment this has several disadvantages. Silicon devices, for example, have a negligible reverse current at room temperature (millimicroamps) and the saturation component of this current is often swamped by the leakage. Furthermore, even on a single batch of devices, there is a considerable spread in I_{CBO}, so that each device must be individually calibrated. Finally, it has been noted that the reverse current often tends to vary with time.

Nelson and Iwersen (Ref. 5) used the variation in forward current gain to determine the temperature rise in large-area diffused devices. However, this method will not necessarily be suitable for all transistors, and it cannot be applied to diodes.

For a general-purpose equipment the temperature-sensitive parameter used is that of a forward biased diode. Roberts and Scarr (Ref. 6) describe a method that uses the change in current for a constant input voltage, while Lin and Crosby (Ref. 7) and Simmonds (Ref. 8) use the change in input voltage for a constant current. Gates and Johnson (Ref. 9) also favour the latter, and it is a method using this parameter that will be described in the next section.

An advantage of this parameter is that, by means of suitable switching, either the emitter-base junction or collector-base junction may be forward biased as a diode during the measuring period, so that both junctions may be examined.

Power Measurements

The heat in the semiconductor is the energy of the crystal lattice vibrations. This may be considered as being composed of discrete quanta (phonons) which are uncharged masses moving with random thermal energy. Phonons are generated in two ways: by the motion of a carrier affecting the lattice, considered as joule heating, and by recombination, when the excess energy is radiated as lattice waves.

All internal heating will affect the junction temperature, therefore the junction should not be regarded as the sole heat source. In a diode, for example, not only does joule heating occur throughout the crystal, but also (when the minority carrier diffusion length is great) most of the recombination occurs not in the region of the junction but at the base electrode. For practical purposes a diode is regarded as a black box with an effective source dissipation given by the product of the voltage across the device (V_F) and the current flowing through it (I_F) under steady-state conditions. That is, the diode dissipation is

$$P_F = V_F . I_F. \qquad \ldots(2)$$

Similarly, if a transistor is regarded as a black box, the overall source dissipation is:

$$\begin{aligned} P_S &= V_{CB}.I_C + V_{EB}.I_E \\ &= V_{CB}.I_C + V_{EB}.I_C + V_{EB}.I_B \\ &= V_{EC}.I_C + V_{EB}.I_B. \qquad \ldots(3) \end{aligned}$$

If the operating conditions are such that $I_c \gg I_B$ and $V_{CB} \gg V_{EB}$, the term $V_{EB}.I_B$ may be neglected. Then, to a close approximation, the dissipation is given by two meter readings; thus

$$P_S = V_{EC}.I_C. \qquad \ldots(4)$$

If $V_{CB} \gg V_{EB}$, this expression may be further reduced to:

$$P_S = V_{CB}.I_C. \qquad \ldots(4a)$$

Basic Procedures

There are three methods of determining thermal resistance by the correlation of dissipation and temperature rise. In all three it is assumed that with no dissipation the junction temperature t_j is the same as the reference temperature t_r.

(i) The dissipation is adjusted to give a specified temperature rise. Thus:
  (a) With no dissipation, at a reference temperature t_1, the initial value X_1 of the temperature-sensitive parameter (T.S.P.) is observed.
  (b) With no dissipation, and at a higher reference temperature t_2, the new value X_2 of the T.S.P. is observed.
  (c) At the original reference temperature t_1, a dissipation which will produce the value X_2 of the T.S.P. is introduced, corresponding to the temperature rise $t_2 - t_1$.

(ii) The reference temperature is adjusted to correspond to a specified dissipation. Thus:
  (a) With no dissipation, and at a reference temperature t_1, the value X_1 of the T.S.P. is observed.
  (b) With a known dissipation, and at the reference temperature t_1, the new value X_2 of the T.S.P. is observed.
  (c) With no dissipation, the reference temperature is adjusted to produce the value X_2 of the T.S.P.

(iii) When the temperature-stabilisation time of the device is long, the above methods are very time-consuming. Therefore when the T.S.P. is linear over the expected temperature range, the simplest method is to perform a prior calibration of the T.S.P., as in steps i (a) and i (b). From this calibration, the change in the T.S.P. produced by a known dissipation, as in ii (a) and ii (b), may be converted to the change in temperature of the source.

MEASURING APPARATUS

The basic principle, applied in the simplest case to a diode, is as follows. A small constant current (the reference or standing current) is passed through the device under test to provide a reference voltage V_{ref} at the initial junction temperature t_{j1}. Then a further current, which will result in a known constant dissipation $V_F . I_F$, is switched into the device. At the end of a period sufficient to ensure that stable temperature conditions are reached, the dissipating current is cut off, and the value of the forward reference voltage at the new junction temperature t_{j2} is recorded. The change in forward voltage, correlated with a prior calibration against temperature, enables the relevant temperature rise $t_{j2} - t_{j1}$ to be assessed. From a knowledge of the dissipation and the resultant temperature change, the thermal resistance may be calculated.

The method is 'one-shot'; but this has two major disadvantages. A complex monitoring system (for example, a storage oscilloscope) will be required to record the transient change in forward voltage; and a succession of measurements, each with an increased dissipating period, is required to verify that the stable temperature state has been reached.

By means of a repetitive pulse and an oscilloscope display, both these disadvantages are overcome. When an oscilloscope is used to display the forward voltage waveform, the stable state is clearly indicated when no further change in the level of forward voltage waveform is observed. From Fig. 3 it may be seen that, basically, we are measuring ΔV. This is the difference between two d.c. levels: the forward voltage at t_{j1}, and the forward voltage at t_{j2}. Therefore direct coupling must be used to the indicator. If the oscilloscope is used as the measuring instrument, and a very large Y shift (backing-off voltage) is not available, then the sensitivity range of the instrument is reduced by the presence of the large standing voltage produced by the reference current. Even if such shift facilities are available, it is necessary to use a highly accurate and sensitive instrument to provide the required measuring accuracy, as a typical change in the forward voltage of a constant-current biased junction is only −2mV/degC.

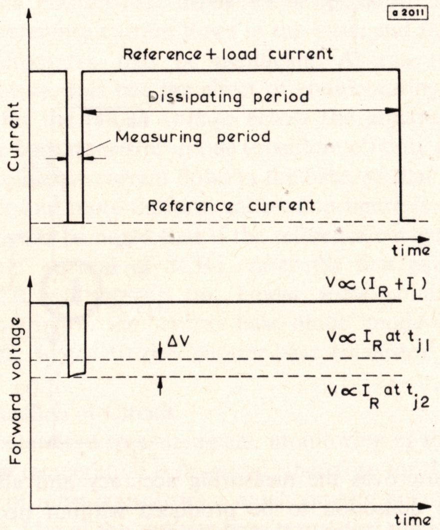


Fig. 3—Basic current and voltage waveforms, where $t_{j2} - t_{j1} = P\theta$

The necessity for a high-grade instrument has been avoided by using the oscilloscope merely as a null indicating device in conjunction with an amplifier. The amplifying

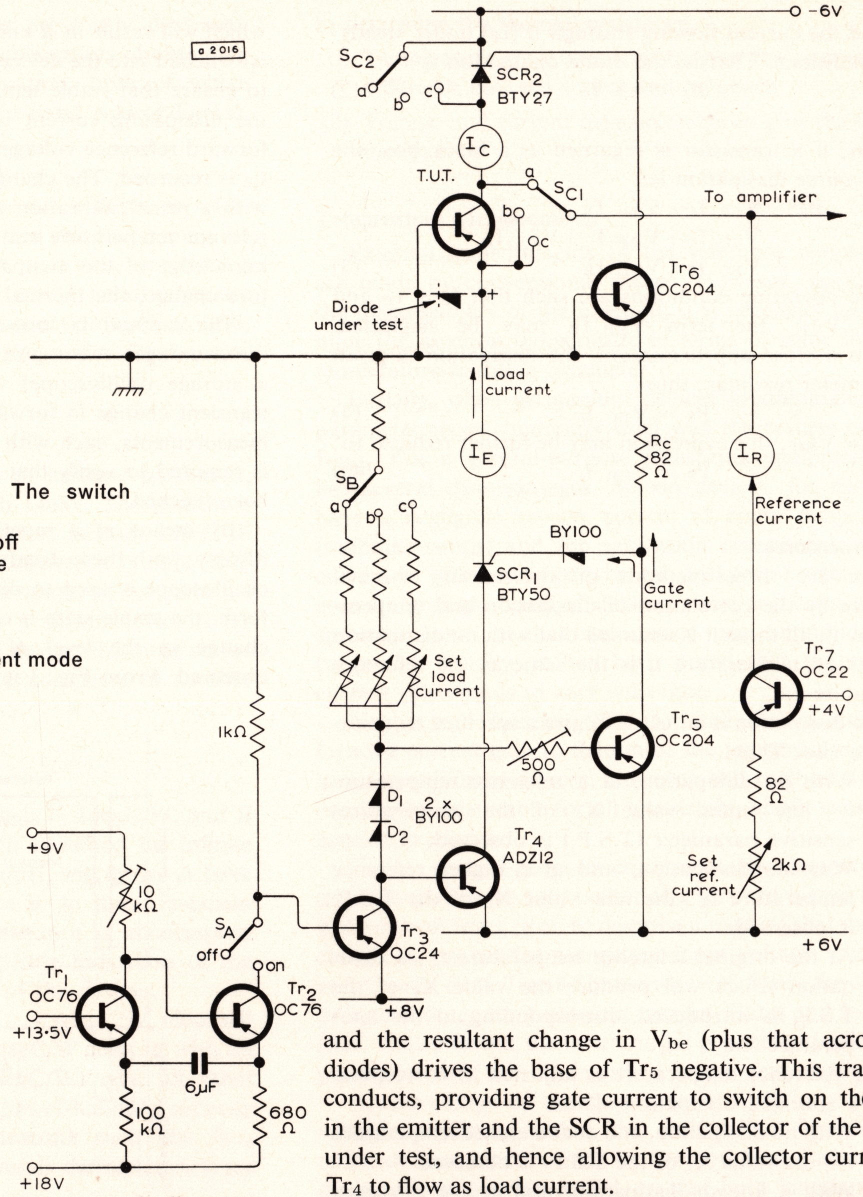


Fig. 4—Current-switching circuit. The switch functions are:
S$_A$: 'dissipate' on and off
S$_B$: load-current range
(*a*) 10mA to 300mA
(*b*) 300mA to 3A
(*c*) 3A to 15A
S$_{C1}$/S$_{C2}$ (ganged): measurement mode
(*a*) V$_{eb}$ as diode
(*b*) V$_{eb}$ as diode
(*c*) V$_{eb}$ as transistor

facility improves the measuring accuracy and allows an adequate deflection to be produced without necessarily applying the maximum permissible dissipation to the device.

Basic Operation of Circuit

The current-switching circuit is shown in Fig. 4. With the 'dissipate' switch S$_A$ off, sufficient base current flows in the high-gain transistor OC24 (Tr$_3$) to bottom this device with all possible values of collector load. Consequently the base of the main switching transistor (Tr$_4$) and that of the gate switching transistor (Tr$_5$) are held positive with respect to their emitters. Under these conditions, no load current flows and the reference current and amplifier may therefore be set up.

Transistors Tr$_1$ and Tr$_2$ form a simple emitter-coupled multivibrator. With the 'dissipate' switch on (during the main period when Tr$_2$ is conducting) the base of Tr$_3$ is driven positive with respect to its emitter, thereby cutting the device off. A base current as defined by the variable base resistor now flows in the switching transistor (Tr$_4$) and the resultant change in V_{be} (plus that across the diodes) drives the base of Tr$_5$ negative. This transistor conducts, providing gate current to switch on the SCR in the emitter and the SCR in the collector of the device under test, and hence allowing the collector current of Tr$_4$ to flow as load current.

During the brief period when Tr$_2$ is cut off, Tr$_3$ cuts on and, by bottoming, cuts Tr$_4$ and Tr$_5$ off. The current through both SCRs now falls below the 'hold' value, so that they are cut off, and only the reference current flows. The change in forward voltage of the device under test is observed during these periods.

The major disadvantage of this fully-transistorised system of switching is that the equipment is suitable for measuring only one type of device. Two equipments are necessary, one for p-n-p and the other for n-p-n devices.

Load Current Setting

The load current is the collector current of the switching transistor (Tr$_4$) plus the gate current of SCR$_1$. Except at low current levels, the gate current is small enough to be ignored. The load current may be defined either in the emitter or the base of the switching transistor.

The disadvantages of defining the emitter current are that only discrete levels of current can be produced by switching emitter resistors, that high-wattage components are necessary at the higher current levels, and furthermore a larger input signal to the switching transistor and higher voltage rails are required.

The main disadvantage of defining the base current is that the load current is not as temperature-stable as with emitter definition. However, as any drift in load current can be seen and corrected for, this method was used. A range switch selects the relevant variable resistor, and by using a common shaft a single 'set current' control is possible. The load current ranges are approximately 10mA to 300mA, 300mA to 3A, and 3A to 15A. The base resistor values are governed mainly by the gain of the switching transistor, and also to some extent by the base current drawn by the SCR gating transistor.

The equipment has its own internal 3A emitter and collector supplies, but for testing power diodes provision is made to connect an external 6V high-current supply. If the voltage rails are slightly reduced, the whole equipment can be operated from a 12V accumulator and dry batteries.

Load Current Switching: Diode under Test

As shown in Fig. 3, the reference current always flows through the diode with the load current superimposed. The diode under test is placed in the emitter (+ve) and base (−ve) terminals, and the load current is switched via Tr$_4$ and SCR$_1$.

In order to handle power diodes a load current of 10 to 15A is required. For switching at these levels a high-current transistor is necessary, which unfortunately has a correspondingly large value of leakage current.

A very low level of leakage current is obtained by placing SCR$_1$ in the collector circuit of the switching transistor Tr$_4$. If the transistor leakage current is kept below the 'hold' current of the SCR, the latter will cut off at the start of the measuring period. As the 'hold' current is in milliamps, the comparatively high leakage of the germanium device ADZ12 may be tolerated.

The leakage current is now determined by the SCR. When the SCR is cut off this is negligible (μA), provided that the gate-switching circuit does not allow a considerable current to flow through the device via the gate. The gate current is therefore switched by a silicon device (OC204) which is reverse biased during the measuring period, so that only I_{CBO} flows.

Load Current Switching: Transistor under Test

When measuring thermal resistance, it is essential to dissipate the device as a transistor to simulate normal operating conditions. Hence the following switching operations are required to monitor either junction as a forward biased diode

(i) during the dissipating period both emitter and collector are connected as for normal transistor operation
(ii) at the start of the measuring period both emitter and collector circuits are broken
(iii) then either emitter or collector is connected to the constant current source to act as the forward biased diode.

The 'emitter open circuit' condition is satisfied by using SCR$_1$ in the emitter current source of the transistor under test. The 'collector open circuit' condition is achieved by the use of a second device SCR$_2$ in the collector circuit, which is gated simultaneously with SCR$_1$. When the load current is switched off, the current in both SCRs falls below the 'hold' value, and both cut off and provide effective open circuits.

When monitoring the collector junction the collector is connected to the reference current source (position 'a' of S$_{C1}$). During the dissipating period both load and reference currents flow via SCR$_2$ to the negative rail. During the measuring period the reference current will flow to earth via the collector-base diode. Alternatively, if the reference current source is connected to the emitter (positions 'b' and 'c' of S$_{C1}$), when the collector is 'open circuit' the emitter-base junction will act as the forward biased diode.

Provision is also made to short-circuit the SCR in the collector, so that the collector is connected during both the dissipating and measuring periods. In this configuration the collector junction cannot be measured as a forward biased diode, but the emitter junction may be monitored as the V_{eb} of a transistor. Alternatively, this may be regarded as measuring the variation of h_{IB} (the static value of the input resistance) with temperature.

In the 'emitter-base diode' mode (position 'b' of S$_{C2}$) all the reference current flows in the base, and the voltage drop across $r_{bb'}$ may be significant. As $r_{bb'}$ rises with temperature, this has the effect of compensating to some extent for the fall in voltage across the junction. In the 'emitter-base transistor' mode (position 'c') only a fraction of the reference current flows in the base, so that generally a higher and more uniform calibration figure is obtained.

It should be noted that if the reference current exceeds the 'hold' current of SCR$_2$, after the first gating cycle this SCR will remain on. Under these conditions an initial setting in the 'emitter-base diode' mode will automatically switch to the 'emitter-base transistor' mode.

Simplification of Circuit

For standard measurements, monitoring of the emitter junction temperature is favoured; therefore for the routine testing of most transistors a much simpler circuit may be evolved. Use of the 'emitter-base transistor' mode obviates the necessity for a collector SCR, and has the advantage of a uniform calibration figure. By reducing the current level that is switched into the emitter of the transistor under test, both the maximum current rating and the dissipation in the switching transistor may be reduced.

At a maximum current level of approximately 1A it should be possible to operate with such a low level of leakage current that the emitter SCR is also unnecessary. With a power device under test, a current of 1A can produce adequate dissipation, provided that V_{eb} is sufficiently high.

Silicon Controlled Rectifier Gating

A silicon device is required as the gating transistor (Tr$_5$) of the emitter SCR to ensure that a negligible gate current flows during the measuring period. A larger voltage change than that provided by the emitter-base diode of the germanium switching transistor (Tr$_4$) is therefore necessary to cut the device on. The two silicon diodes (D_1 and D_2) produce a more than adequate input to Tr$_5$, and a preset resistor is used to limit the base current. With two diodes the overall variation in the forward voltage (of the diodes and Tr$_4$) with load current is comparatively small, so that excessive overdrive to Tr$_5$ is avoided at high load current levels.

The load impedance presented to Tr$_5$ by the device under test and the gate of the emitter SCR$_1$, is not constant, so that the value of the parallel load resistor R_c is a compromise. It must be low enough to ensure that the component of Tr$_5$ collector current (V_{Rc}/R_c) that flows into Tr$_6$ is sufficient to gate the collector SCR when the emitter SCR path presents a low impedance (that is, with no meter and small forward voltage of the device under test), and yet not so low as to starve the emitter SCR gate when this path presents a high impedance.

The larger the overall gate current provided by Tr$_5$, the faster the switching of the SCRs, but the higher the dissipation in Tr$_5$. Although Tr$_5$ has a heatsink to minimise the junction temperature rise, the base resistor is preset so that the minimum gate current requirements are met at the lowest load current levels. Any consequent overdrive of Tr$_5$ at high load currents will increase the gate current and provide faster switching, without producing excessive dissipation. Furthermore, as larger reference currents are used at high load levels, any consequent increase in the leakage of Tr$_5$ with temperature can be tolerated.

Reference Current

The rise in junction temperature is assessed from the fall in the forward voltage level at a given reference current. As the forward voltage is a function of both current and temperature, it is essential that the current remains constant.

Since there is a change in the forward voltage of the device under test (ΔV) during measurement, the reference current source must have a very high output impedance. This could be achieved by a large series resistor and a high-voltage rail; but rather than making special provision for an h.t. supply, a common-base stage Tr$_7$ (Fig. 4) is used, operating from the existing voltage rails. With the high output impedance of this configuration, a change in collector voltage ΔV of approximately 100mV will result in a change of only a few microamps in the initial reference current.

As Tr$_7$ is a power device on a large heatsink, at the low reference levels that are used the corresponding junction temperature change of this device is less than 1degC. Consequently, the change in the emitter-base voltage with temperature is negligible (1 to 2mV) so that the emitter current as defined by R_E remains constant; furthermore, variations in collector current caused by changes in leakage current and current gain with temperature are minimised.

The variable emitter resistor allows the reference current to be set between 1 and 20mA, in which range the circuit may be regarded as a constant current source. In general, the standard values of reference current (I_R) used are 1mA for low- and 10mA for high-power devices. These values, while being much lower than the corresponding dissipating currents, are nevertheless far greater than the saturation current I_s of the device under test (I_R/I_s preferably greater than 1000) so that the change in forward voltage with temperature is substantially linear over a wide temperature range.

Amplifier and Null Reading Circuit

If the input voltage e_i to the simple common-base amplifier circuit of Fig. 5 falls by an amount ΔV, then, by reducing the base voltage by an equal amount, the initial current conditions of the transistor are restored and the collector voltage returns to its initial level. If the output e_o from the collector is applied to an oscilloscope, this may be used as a null indicator, and the change in input voltage may be measured directly by a d.c. meter as the corresponding change in base voltage.

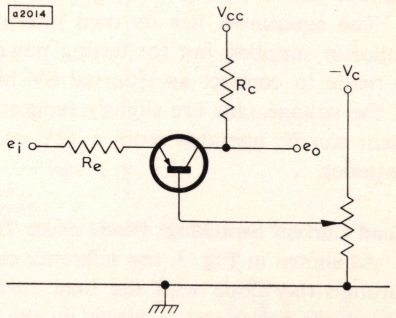


Fig. 5—Basic amplifier circuit

Set Amplifier Control

In the practical circuit of Fig. 6, the 'set amplifier' control provides a variable base voltage of 0 to -1V. This coarse control enables the amplifier output to be set to approximately -1V with respect to earth over a very wide range of initial input voltages. A standard value of -1V at the output is chosen arbitrarily as being generally just out of bottoming and not producing an excessive standing voltage to be backed off on the oscilloscope.

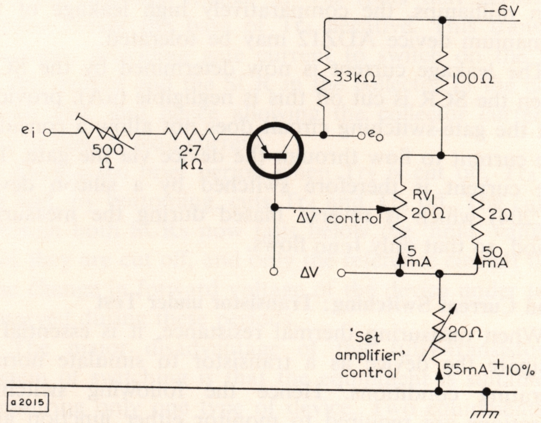


Fig. 6—Practical null-reading circuit

ΔV Control

The ΔV control is the fine base voltage control, used to back off the waveform to the initial reference level. It consists of a fixed resistor (2Ω) in parallel with a potentiometer (20Ω). With a 50mA current in the backing-off chain this gives a maximum ΔV of approximately 100mV, which allows for a maximum temperature change of 50degC (assuming -2mV/degC). The potentiometer enables ΔV to be set from 0 to 100mV to within 1mV (that is, 1% of full scale). For power devices a power level which gives a minimum temperature rise of 15degC is tolerated. In this limit, 1mV now represents a 3% setting accuracy, but with normal resolution of the displayed waveform this is generally adequate. Resolution may be improved by increasing the amplification and setting accuracy by reducing RV$_1$.

The change in forward voltage, as indicated by the fine base voltage control ΔV, is not with respect to earth. A floating high-impedance valve-voltmeter is therefore required to monitor this d.c. voltage.

Amplification

With a typical oscilloscope sensitivity of 100mV/cm, a change of 1mV represents 0·01cm with no amplification. Adequate resolution requires at least 0·1cm for 1mV change in ΔV (that is, an amplification of 10). For all practical purposes $I_c = I_e$, so that the voltage amplification is determined by the ratio R_c/R_e.

The advantage of a large value of R_e is that the loading effect on the device under test is small; but this has the disadvantage that the corresponding large value of R_c, in conjunction with the output capacitance of the amplifying transistor, will produce a long response time. Typical compromise values of $R_e \simeq 3\mathrm{k}\Omega$ and $R_c \simeq 30\mathrm{k}\Omega$ are used.

With the null technique the actual gain is not of prime importance, but the preset emitter resistor may be used to adjust the gain, thereby facilitating calibration of the oscilloscope in terms of ΔV if this is required.

Operation

The constant current passed through the device under test produces an initial positive reference voltage $V_{in(R)}$ with respect to earth. This voltage is applied to the amplifier and, with the ΔV control at zero, the 'set amplifier' control is adjusted to give a new negative reference voltage $V_{out(R)}$ at the collector (approximately -1V). During the dissipating period the input voltage rises below $V_{in(R)}$ and drives the amplifier into bottoming. During the measuring period, as a result of the junction temperature rise, the input voltage will be below $V_{in(R)}$ and the collector will be driven towards the negative rail. The overall waveform as displayed on the oscilloscope is as shown in Fig. 7a.

The change in base voltage of ΔV which raises the lower level of the waveform to the original reference (Fig. 7b) gives a direct indication of the corresponding change in forward voltage of the device under test.

Intrinsic Errors in the ΔV Reading

In order to produce a reference voltage of -1V from the -6V rail, a collector current of 150μA is required. With a current gain $\beta = 20$ the corresponding base current is negligible compared with the 5mA through the potentiometer RV$_1$. However, during the main dissipating period when the amplifier bottoms, a larger base current will flow through RV$_1$ and produce a spurious voltage across the lower arm. Because of the large duty cycle, the mean reading of the valve-voltmeter is the spurious value.

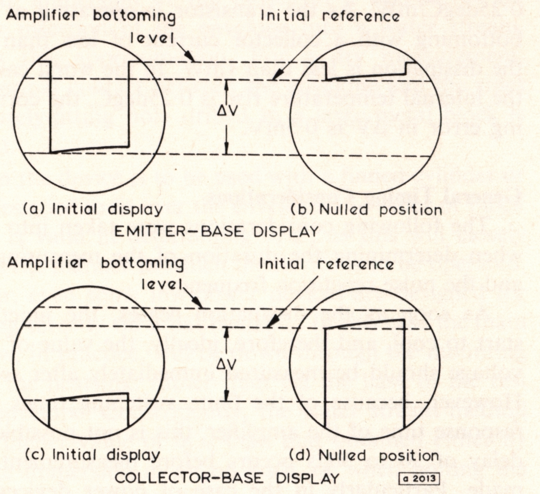


Fig. 7—Oscilloscope display

The error is not always significant. Even with a large rise in input voltage of say 600mV, with $R_e = 3\mathrm{k}\Omega$ the base current of 200μA will result in an error of only 0·5% at the maximum setting of ΔV. At the minimum setting of ΔV, however, with a comparable change, the error rises to 4% (see Appendix, page 140). This error may be reduced at the expense of amplification by increasing R_e, but in all cases the true value of ΔV may be obtained by switching the 'dissipate' switch off.

Indicator Errors

Any simple d.c. oscilloscope with a sensitivity of 100mV/cm may be used as the null indicator. A possible source of ΔV error is the spurious d.c. shift produced by unbalanced outputs from the oscilloscope amplifiers. Any such inherent error may be revealed by inserting a resistor as the device under test when, as ΔV is zero, any shift is spurious.

The bottoming action of the amplifier provides positive limiting of the oscilloscope input. However, if the amplifier is also to be used for monitoring the collector-base diode, a very large amplitude output from the amplifier will result: from -1V when measuring, to -6V when dissipating. A diode limiting circuit taken to -2V will prevent this heavy overload from producing spurious d.c. shift.

Temperature Errors

The ΔV control will also indicate any change in the emitter-base voltage of the amplifier. As this is a temperature-sensitive parameter, ideally no change in junction temperature should occur.

The copper block in which the transistor is mounted is effectively an infinite heatsink, and its large thermal capacity screens the junction from any sudden or short-term variations in the ambient temperature. Furthermore, it reduces the thermal resistance to its internal value of

0·25degC/mW. As the transistor is operating at or near bottoming with a collector current of less than 200μA, the dissipation is less than 1mW. In the worst case, when the internal temperature rise is 0·25degC, the corresponding error in ΔV is 0·5mV.

General Timing Considerations

The following considerations were taken into account when determining the duration of the measuring period and the pulse repetition frequency.

As soon as the dissipation ceases, the junction will start to cool, and therefore, ideally, the value of forward voltage should be measured immediately after switching. However, because of the finite switching times and the response time of the amplifier, this is not possible, and a delay of 20 to 50μs occurs before measurement can be made. Particularly in the case of power devices, where large currents are being rapidly switched, spurious transients are likely to occur after switching; and with very short measuring periods there is no method of discerning such effects. However, if the measuring period is sufficiently extended, any spurious transient can be seen as a discontinuity in the general cooling curve. Within a measuring period of 1 to 2ms, sufficient cooling normally occurs to indicate whether the cooling waveform is purely thermal or partly spurious. When in doubt, measurement is made after a standard delay of 200μs on the assumptions that by this time spurious effects are negligible and errors due to cooling are only 2 to 3%.

In order that steady-state conditions shall be effectively maintained, the measuring period in which the junction cools should be negligible compared to the dissipating period. By using a dissipating duty cycle of about 200:1 this is realised. With a measuring period of 1ms this gives an overall period of 200ms; that is, a resultant p.r.f. of 5c/s.

By ensuring such a long duty period, the difference between the peak values (occurring during dissipation) and the average values (as recorded by d.c. meters) is only 0·5%. Therefore any error in calculating the dissipation, as indicated by the readings of d.c. instruments, is governed by the accuracy of the instruments.

PRACTICAL MEASURING CONSIDERATIONS

Earlier sections of this article have discussed the theoretical background of heat transfer, the principles of thermal resistance measurement, and a general-purpose measuring circuit. In this section we shall discuss the practical aspects of thermal resistance measurement, which may be considered under two headings: temperature monitoring, and the establishment of the required dissipation conditions.

Temperature Monitoring: Internal Temperature Measurements

The junction temperature is derived from measurement of the change in forward voltage at a constant current. The value of ΔV read from the d.c. meter is converted into the corresponding ΔT_j from a prior calibration of this parameter.

Calibration is performed by observing the change in the temperature-sensitive parameter when the junction temperature is varied by external means (that is, by varying the reference temperature).

Stirred oil baths or forced air ovens provide means of calibrating any device irrespective of its encapsulation. A further method suitable for any encapsulation (now being investigated) is the heated fluidised bed (Ref. 8). However, if a temperature gradient exists in the heating medium used in these methods, it is possible that the true case temperature will not be monitored.

The preferred method of varying the reference temperature is by the use of a temperature-controlled block. By mounting the device as a push fit into the block or by bolting it on to the block, the measurement is made clean and rapid, and the temperature is more uniform.

For accurate results, considerable care must be taken, as spurious temperature readings are known to be a major source of error. Instrument inaccuracies are compensated for, as the same equipment is used both to calibrate and to measure the thermal resistance. Operator errors are minimised if it is remembered that adequate time must be allowed for the device to stabilise at each temperature level; this is particularly important at the initial reference, where, if the device has been handled, it must be allowed to cool to the ambient.

A calibration graph may be produced; but, in general, three or four spot measurements indicate whether the changes are consistent with a constant calibration figure.

Temperature Monitoring: External Temperature Measurements

Measurement of the external reference temperature may be made with the following instruments.

Mercury-in-glass thermometer: For a low-power device mounted in free air, or in a liquid (for example, an oil bath), the mercury-in-glass thermometer provides a simple and suitable method. However, placing one side of the bulb in contact with a metal surface, such as the case of a device or a heatsink, is not always reliable since the ambient has a thermal shunting effect.

Thermistors: Various forms of electronic thermometer using a bead thermistor and a directly-calibrated temperature meter are available. Generally, these are accurate to within 1°C over the range 0°C to 100°C. They have the advantage of being rapid and flexible in use. It is not always necessary to drill into the sample to insert the probe; but as the bead will be thermally shunted by the ambient when direct surface measurements are made, screening by grease or Plasticine is necessary to improve the accuracy.

Thermocouples: Thermocouples are generally used when a high degree of accuracy is required, as, for example, in the initial assessment of a device. The Chromel-Alumel thermocouple is most generally used as it is the most reproducible. When making such a thermocouple junction, the wires are not merely twisted together but are spot-welded. In use, the thermocouple is generally inserted into a small hole ($\frac{1}{16}$in dia, $\frac{1}{4}$in deep) specifically drilled for the purpose. Silicon grease is used to improve the contact.

When monitoring temperature, the simplest method is to connect the thermocouple leads directly to a suitable high-impedance valve-voltmeter, in which case the meter terminals form the cold or reference junction. However, particularly in the case of small temperature difference measurements, greater accuracy is obtained by the use of melting ice or an oil bath as the cold junction reference. The advantage of a temperature-controlled oil bath is that the reference temperature may be backed off to improve the meter-reading accuracy. Calibration of the thermocouple may be compared against standard figures (for example, Kaye & Laby). These figures indicate that over the range 20°C to 100°C, the sensitivity is approximately 41μV/degC.

External Temperature Measurements on Low-power Devices

The thermal resistance of high-power devices is normally measured with the device mounted on a heatsink. For low-power devices, however, several values of thermal resistance are of interest:

(i) θ_{j-a} in free air,
(ii) θ_{j-a} with a small specified heatsink,
(iii) θ_{j-c} with an 'infinite' heatsink.

In the case of (i) and (ii) the external component (radiation and convection) depends not only on the dissipation level as previously discussed but also on the mounting conditions, and standardisation is difficult. For the free air value the device is measured under the most adverse conditions; that is, in a draught-free enclosure and with the device held at full lead length. When room temperature is used as the initial reference, care is taken not to handle the device excessively; or, alternatively, sufficient time is allowed for the device to cool down to room temperature before measurements are carried out.

If, on a sample batch of devices, careful measurements are made of their overall thermal resistance (θ_{j-a}) in free air and their internal thermal resistance (θ_{j-c}) on an 'infinite' heatsink, the difference of these two measurements will give a typical value of the external thermal resistance. Adding this value to the measured internal value gives the required overall value for any further samples.

There are several reasons for preferring measurement of the internal thermal resistance:

(i) Mounting on an 'infinite' heatsink considerably reduces the temperature stabilisation time, giving a consequent increase in the speed of measurement.
(ii) The internal temperature range is extended, giving improved sensitivity.
(iii) Convection and radiation effects are negligible, and better repeatability of results is obtained.
(iv) In its own right, the internal thermal resistance measurement indicates the maximum power-handling capacity of the device.

For the measurement of internal thermal resistance a close approximation to the infinite heatsink is desirable. Complete immersion of the device in a well-stirred oil bath, or insertion of the envelope into a water stream, provides this approximation. For a dry measurement, good thermal contact between the envelope and the sides of a closely-fitting hole drilled in a large metal block is sufficient.

When the device is to be used with a finned cylinder or a flag, designed to fit over the envelope, the water or block method is valid in determining θ_{j-c}, as this will closely simulate the manner in which the device is to be operated. However, even some low-power devices are designed for mounting directly on a flat heatsink. In this case the main heat flow, in practice, will be down through the mounting base to the heatsink, rather than via the base to the rest of the envelope. Consequently, the water stream method gives a higher value of θ_{j-c} than that obtained either by complete immersion in an oil bath, or when bolting the device down to a heatsink.

With these low-power devices, variations in the initial reference temperature are insignificant. It is not necessary to determine the absolute values of reference and junction temperatures, as only their difference is required. This, of course, assumes that the calibration of the temperature-sensitive parameter is constant over the measurement range.

External Temperature Measurements on High-power Devices

With high-power transistors, the internal thermal resistance is low, and the overall value θ_{j-a} is very dependent on the heatsink. Therefore only the internal value (junction to mounting base or junction to stud) is quoted. With the hypothetical infinite heatsink, no measurement of external reference temperature is really necessary; for, even if unknown, it is nevertheless constant, and it is a change which is monitored.

In practice, the heatsink is finite and there is also an interface contact thermal resistance; so that, when power is dissipated in a device, the junction, the case, and the heatsink temperatures all rise with respect to the initial reference. Consequently the internal thermal resistance cannot be measured directly, but must be found as the difference of two measurements. If the case temperature is monitored, not only θ_{j-a} but also θ_{c-a} may be determined, giving

$$\theta_{j-c} = \theta_{j-a} - \theta_{c-a}.$$

With normal measuring accuracies (say 5%) a large value of θ_{c-a} (such that $\theta_{j-a} \simeq \theta_{c-a}$) will produce a large inaccuracy in θ_{j-c}. A close approximation to the infinite heatsink is therefore desirable.

The stirred oil bath immediately suggests itself; but for power transistors designed for mounting on a plane surface, typical operating conditions are not realised, since the whole surface area of the case is used for heat transference. Furthermore, even if the possible temperature gradients in the oil adjacent to the case are neglected, the method is rather inconvenient.

A better method is to use a large plate of good conducting material; for example, copper with water cooling. Careful machining of the heatsink surface is necessary to keep the contact thermal resistance low. However, as some thermal resistance exists between case and reference, even assuming a constant reference, it is generally essential to monitor the case temperature.

By drilling a small hole in the stud or mounting base into which a thermocouple may be inserted, an accurate determination of its temperature can be obtained. There are two simpler but less accurate methods.

(i) The thermocouple of an electronic thermometer probe may be placed on the mounting base. (The thermal contact is improved with silicon grease.)

(ii) A thin blank of copper, conforming to the device outline, is inserted between the device and the heatsink. On the assumption that there is negligible interface thermal resistance between the blank and the test device, a thermocouple in the blank indicates the mounting base temperature.

Monitoring of the case temperature is not necessary on large-scale testing in the following instances.

(i) For high-power devices the internal thermal resistance is 1degC/W or less, and a low value of contact thermal resistance is essential. These devices have an extremely well-finished mounting base, and for stud-mounted devices a specified torque is generally given. Under these conditions a comparatively uniform value of contact thermal resistance may be obtained; and with a known heatsink the measurement is considerably simplified by measuring the overall thermal resistance and allowing for a constant value of external thermal resistance.

(ii) For low-power devices with a higher value of thermal resistance (for example, greater than 3degC/W), the contact thermal resistance is not so significant. It may either be neglected, or on a GO-NO GO test can be compensated for by increasing the maximum permissible value of overall thermal resistance by a standard amount.

In both instances, accurate measurements must be made on a few initial samples to determine the value of contact and heatsink thermal resistance.

Dissipating Conditions

Dissipating Level

When the device is mounted in free air, the heat transfer from the envelope via convection and radiation must be considered. As both are proportional to the temperature difference between envelope and ambient, there will be a decrease in the external thermal resistance as the dissipation increases.

When the internal value is much greater than the external value, any increase in dissipation will produce a correspondingly small increase in the external temperature difference. The resultant small change in the external value will be negligible compared to the overall value. It usually lies within the measuring accuracy of the equipment, making variations in thermal resistance with power hard to detect.

However, as the published data value is that for the device under the most adverse conditions, the dissipating level should be the minimum (lowest convection and radiation) that gives good reading accuracy. A dissipation that results in a temperature change of 30degC±5degC is generally used.

For a power device bolted to a heatsink, or in any other instance where the internal thermal resistance is being determined, the heat transfer is predominantly by conduction. The dissipating level is therefore relatively unimportant, since all that is required is a readable change in forward voltage. As higher dissipating levels are required in power devices, a minimum temperature change of 10degC to 15degC is tolerated.

In some instances it may be found that the calibration figure is not constant over the whole temperature range; therefore care must be taken that the figure used is relevant for the junction temperature change produced by the dissipation. Where non-linearity exists, it is the calibration accuracy that governs the relevant dissipation level measurements. For example, if we assume that an overall error of 1degC is possible in taking two temperatures, this would be equivalent to a 6% calibration error in 15degC, but only 3% in 30degC. Therefore a higher dissipation, by increasing the calibration range, would give a more accurate indication of the relevant temperature change.

Normal Operating Conditions

In order to produce the normal heat generation in a transistor it is necessary to dissipate the device as a transistor and not as a diode. This can be illustrated by an example.

Let us assume 100mW dissipation is required in a low-power device. Then $V_{CE} = 5V$, $I_c = 20mA$, would simulate typical working conditions; and with a β of 50 the corresponding $I_B = 0{\cdot}4mA$. Now, merely using the collector and base as a diode would require, for $V_{CB} = 0{\cdot}5$ to 1V, a corresponding high forward current of 100 to 200mA. At this high current level, abnormally high joule heating will occur in the material, extensive recombination could occur at the base contact, and more electron recombination in the emitter. All these factors will tend to alter the effective heat source position in the device, thereby modifying the internal resistance paths.

Errors in Calculating Dissipation

For a diode, the dissipation is given by $V_F.I_F$. This assumes that either the standing current is not being measured, or that it is sufficiently small to be neglected.

When using flying leads to connect from the equipment to a device on an adjoining heatsink, care must be taken, particularly with germanium diodes. At high current levels, an overall voltage drop in the leads of 30mV may be an additional 5 to 10% of the voltage across the device. Therefore additional voltage monitoring leads may be essential to ensure measurement of the true forward voltage across the device.

For a transistor, the dissipation is generally calculated as $V_{CE}.I_C$, since this expression requires only one voltage and one current reading. There is an error in ignoring the component $V_{EB}.I_B$; but the error is significant only at very high current levels, where the fall in α results in a large base current, or if V_{EB} is comparable to V_{CB}. Any drastic fall in β at high current levels will give not only an error in calculating P_{ce} (which may be corrected for); but, by increasing base recombination or the electronic recombination in the emitter, it will also alter the effective heating.

In normal transistor operation, and particularly for measuring purposes, V_{CB} is greater than V_{EB}. Indeed, if V_{CB} is made far greater than V_{EB}, the dissipation may be further approximated to $V_{CB}.I_C$. The use of this dissipation figure for a measured temperature change will result in a slightly higher and therefore safer value of quoted thermal resistance.

In both emitter-base diode and transistor configurations, the value of I_c used in determining the dissipation is the change in the collector current meter reading between 'dissipate on' and 'dissipate off'; that is, from 0 to I_L in the emitter-base diode configuration, and from I_R to $I_R + I_L$ in the transistor configuration. However, in the collector-base diode configuration, as the reference current is diverted through the collector current meter without heating the device in the dissipating periods, and as the value of I_c with 'dissipate off' is zero, the relevant current is $I_L - I_R$. These factors are only considered when using low load-current levels; in all other instances, when I_L is far greater than I_R, no such correction is necessary.

SUMMARY OF METHOD

The thermal resistance measuring equipment described has been designed as a general-purpose gear for laboratory use. Hence a very wide current range is provided, and the load current is switched so that either the emitter or collector junctions can be monitored.

It is now generally considered that the emitter junction gives the more accurate indication of temperature, so that collector switching is not essential for routine testing. At low current levels, where the leakage current of the switching transistor may be neglected, the emitter SCR can also be omitted. A far simpler circuit has been evolved for n-p-n transistors which monitors only the emitter junction. The battery-operated prototype now in use has no SCRs and merely uses a 1A silicon transistor.

With both equipments an oscilloscope is used as a null indicator, and the change in forward voltage (the temperature-sensitive parameter) is read from a d.c. valve voltmeter.

PRECAUTIONS

The following points summarise some of the difficulties and possible errors that may arise in practical measurement.

Dissipation Errors: A known error is introduced by calculating the dissipation from two meter readings $V_{CE}.I_C$. However, the operating conditions are assumed to be such that the error in ignoring the component $V_{EB}.I_B$ is negligible. A possible operator error lies in ignoring the effect of the reference current; the significance depends on the ratio load current/reference current.

Errors in Forward Voltage: With a large input heavily bottoming the amplifier, an operator error arises in measuring the change in forward voltage (ΔV) while the 'dissipation' switch is on. With a spurious switching transient, ΔV cannot be monitored immediately, so that cooling occurs; however, even without extrapolation, the assessed error on power devices is only 2% to 3% if a delay of 200μs is used. As the ΔV setting is 1mV, a dissipation producing a minimum change of 30mV (approximately equal to 15degC) is desirable.

Calibration Errors: Instrument errors are largely compensated for by calibrating and measuring on the same equipment. A possible source of error is in not allowing the junction sufficient time to reach the reference temperature. Further errors may arise in the positioning and reading of the temperature indicator.

Mounting: The thermal resistance of a device is not unique but depends on the mounting. Where possible, the mounting during measurement should simulate that which will be used in practice. Measurements made on devices with heatsinks are more easily standardised and are used wherever possible.

The internal thermal resistance (θ_{j-c}) is determined as the difference between the overall value (θ_{j-a}) and the external value (θ_{c-a}). Errors are minimised if the external value is kept as low as possible by using a large plate or a water-cooled heatsink and by ensuring a low interface thermal resistance. Under these conditions, errors in monitoring the case temperature are less significant.

With an effective 'infinite' heatsink there is a much shorter temperature stabilisation time. As the measurement may be rapidly repeated, the taking of an average of several readings becomes practicable.

REFERENCES

1. 'IRE Standards on Solid-state Devices: Definition of Semiconductor Terms, 1960'. **Proc. I.R.E.,** Vol. 48, No 10, Oct. 1960, pp. 1772 to 1775.
2. 'Letter Symbols for Light-current Semiconductor Devices'. British Standard 3363:1961.
3. Edwards, O. J. 'Heat Sink Design'. **Mullard Technical Communications,** Vol. 3, No. 29, Mar. 1958, pp. 258 to 264.
4. Tuley, J. H. 'Design of Cooling Fins for Silicon Power Rectifiers'. **Mullard Technical Communications,** Vol. 5, No. 44, June 1960, pp. 118 to 130.
5. Nelson, T. J. and Iwersen, J. E., 'Measurement of Internal Temperature Rise of Transistors'. **Proc. I.R.E.,** Vol. 46, No. 6, June 1958, pp. 1207 to 1208.
6. Roberts, G. N. and Scarr, R. W. A. 'The Design and Measurement of Semiconductor Devices in Terms of Thermal Behaviour.' **Proc. I.E.E.,** Vol. 106 (Part B), Suppl. No. 15: International Convention on Transistors and Associated Semiconductor Devices (May 1959), May 1959, pp. 409 to 418.
7. Lin, H. C. and Crosby, R. E. 'A Determination of Thermal Resistance of Silicon Junction Devices'. **I.R.E. National Convention Record,** Vol. V (1957), Part 3, pp. 22 to 25.
8. Simmonds, C. D. 'Transistor Heat Sinks and their Evaluation'. **Semiconductor Products,** Vol. 1, No. 1, Jan-Feb. 1958, pp. 31 to 33.
9. Gates, R. F. and Johnson, R. A. 'The Measurement of Thermal Resistance: A Recommendation for Standardization'. **Semiconductor Products,** Vol. 2, No. 7, July 1959, pp. 21 to 26.
10. Sutcliffe, H. 'Fluidized Beds as Constant Temperature Enclosures'. **Electronic Engineering,** Vol. 33, No. 396, Feb. 1961, pp. 94 to 95.

APPENDIX

Calculation of error in ΔV

From the voltage between A and E in Fig. 8 we have

$$6 = 100(I_1+I_3)+2(I_1-I_2)+20I_1$$
$$= 122I_1-2I_2+100I_3. \qquad \ldots(A1)$$

From the voltage between B and D we have

$$2(I_1-I_2) = (20-R)(I_3+I_2)+RI_2$$

therefore

$$2I_1 = 22I_2+(20-R)I_3. \qquad \ldots(A2)$$

Substituting in (A1) gives

$$6 = 122\left(11I_2 + \frac{(20-R)}{2}I_3\right)-2I_2+100I_3$$
$$= 1340I_2+(61(20-R)+100)I_3. \qquad \ldots(A3)$$

Now $\Delta V = RI_2$, so that with the value of I_2 obtained from Eq(A3)

$$\Delta V = R\frac{6-I_3(1320-61R)}{1340}.$$

Thus the error introduced in the ΔV reading by the presence of the base current I_3 during the dissipating period, and its much smaller value during the actual measuring period, is

$$\frac{R\Delta I_3(1320-61R)}{1340}$$

where ΔI_3 is the change in the base current. The percentage error is therefore

$$\frac{R\Delta I_3(1320-61R)}{1340}\times\frac{1340}{6R}\cdot 100 = \frac{\Delta I_3(1320-61R)\times 100}{6}.$$

Thus the maximum percentage error occurs when $R = 0$, being $(\Delta I_3/6)132\,000\%$, and when $R = 20$, the percentage error is $(\Delta I_3/6)10\,000\%$.

For a large change in forward voltage between measuring and dissipating periods in the device under test (say 600mV), the increase in base current during dissipation is $0{\cdot}6/3\times 10^3 = 200\mu A$ (since the amplifier is bottomed) and the corresponding percentage errors are

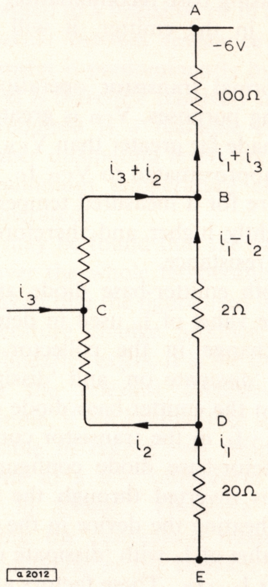
$$\frac{2\times 10^{-4}\times 132\,000\%}{6} = 4{\cdot}4\%$$

at the minimum position of the ΔV potentiometer, and

$$\frac{2\times 10^{-4}\times 10^4}{6} = 0{\cdot}33\%$$

at the maximum position. The error for intermediate positions can be found by linear interpolation.

Fig. 8



Transistorised SCR Firing Circuits

T. J. Jarratt

Mullard Semiconductor Measurement and Application Laboratory

If an SCR is to be fired reliably, the firing circuit used must provide a pulse of sufficient duration and amplitude to meet the requirements of the SCR. As the firing requirements of SCRs vary quite widely, and as the available inputs to the firing circuit may also vary, a range of circuits to cover all possible circumstances is needed.

This article discusses the mode of operation, design procedure and choice of component values for such a range.

INTRODUCTION

An earlier article (Ref. 1) discussed the firing requirements of silicon controlled rectifiers, and recommended that pulse firing should be used wherever possible. Several transistorised circuits for producing these pulses are described in this article.

These circuits are divided into five categories: Pulse Amplifiers, Monostable Circuits, Triggered Blocking Oscillators, Free-running Blocking Oscillators, and Schmitt circuits. Within each category it is possible to choose a circuit which will fire any SCR in the Mullard range.

The circuits discussed here have been designed to operate at ambient temperatures up to 55°C, and incorporate germanium transistors. Where the substitution of silicon transistors would give an improvement in performance, any alterations made necessary by this substitution have been noted.

The choice of circuit for firing an SCR will depend on the voltage or current level of the input to the firing circuit, the type of input (pulse or d.c.) and the output pulse duration required from the firing circuit.

Design examples and practical circuits are given in the Appendix (page 150).

PULSE AMPLIFIERS

A pulse amplifier can be used to fire an SCR when a small-amplitude pulse is available and it is required to use the leading edge of this pulse, after amplification by a single transistor, for firing the SCR. Where the input signal is so small that the output from the single-stage amplifier is insufficient to fire the SCR, another circuit (see Appendix) should be used.

Circuit Operation

Fig. 1 shows an amplifier output stage suitable for firing an SCR. It consists of a transistor fed from a source impedance R_1 and RC-coupled through a series resistance R_s into the SCR gate. The SCR cathode is common with the amplifier earth. By applying a negative input pulse of suitable duration and amplitude, the transistor is bottomed and the voltage to which the output capacitor has charged during the interval between pulses is applied through R_s to the SCR gate. The SCR will fire on the positive-going output pulse, which corresponds to the leading edge of the input pulse. The negative-going output pulse must not exceed the maximum reverse gate voltage rating of the SCR unless a clipping diode is included in the circuit.

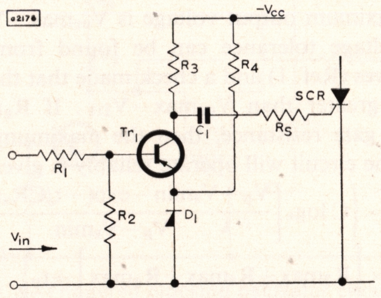


Fig. 1—Pulse amplifier circuit

When there is no pulse input, the transistor is biased off by D_1, R_2 and R_4. Even when the transistor is off, R_4 gives a current of at least 5mA through D_1. The transistor emitter is therefore at a negative potential of at least 0·5V for junction temperatures up to about 60°C. Collector leakage current flows through R_2 and can be considered equal to I_{CBO}.

Circuit Design

Circuit design is concerned with ensuring that sufficient voltage and charge are available to fire the SCR up to a known maximum frequency, with minimum base drive to the transistor.

If the supply voltage is V_{cc}, then at very low frequencies the voltage applied to R_s and the SCR gate will be effectively reduced by the transistor bottoming voltage $V_{ce(sat)}$, the forward voltage drop V_{D1} across the diode D_1, and the voltage drop across R_3 due to I_{CBO}. Thus the minimum initial voltage available for the output pulse V_p is given by

$$V_p = V_{cc}\text{min}-V_{ce(sat)}-V_{D1}-I_{CBO}R_3 \qquad \ldots(1)$$

Since a.c. coupling is used into the SCR gate, the actual voltage pulse applied to R_s and the SCR gate will be a falling exponential. This effectively reduces the voltage available for the pulse to that at the end of the pulse. It has been found adequate to allow a 10% exponential fall during the pulse. Thus the value of coupling capacitor is given by

$$C = \frac{t_p}{R_s\text{min} \log_e 1{\cdot}11} \qquad \ldots(2)$$

where t_p is the minimum output pulse duration required.

To obtain a suitable value of $R_s$min, it is necessary to decide on a value for $V_s$min. As the capacitor charges up exponentially, it will never in theory attain the required voltage, V_p; and as the effect of increasing frequency is to reduce the available charging time, $V_s$min must be considerably less than V_p. In practice, $V_s\text{min} = 0{\cdot}9V_p$ gives pulses of sufficient amplitude over an adequate frequency range.

The maximum value of source resistance ($R_s$max) at which all SCRs will fire reliably is given by

$$R_s\text{max} = \frac{V_s\text{min} - V_1}{i_1} \qquad \ldots(3)$$

where V_1 = minimum voltage to fire all SCRs; and i_1 = minimum current to fire all SCRs.

The maximum output voltage is $V_{cc}\text{max} - V_{D1}$.

The voltage tolerance can be found from the SCR design curves (Ref. 1) and a check made that the allowable $V_s$max is greater than $V_{cc}\text{max} - V_{D1}$. If $R_g$max is the maximum gate resistance, then the maximum frequency at which the circuit will operate reliably is given by

$$f\,\text{max} = \left\{C \log_e\left[\frac{V_p - V_s\text{min} - \exp(-t/CR_s\text{min})}{V_p - V_s\text{min}}\right] \times \right.$$
$$\left. \times \left[R_3\text{max} + R_s\text{max} + R_g\text{max}\right] + t_p\right\}^{-1} \qquad \ldots(4)$$

Maximum current will be required from the output when R_s and R_g are both at a minimum value. The maximum current ever required from the output pulse will therefore be given by

$$I = V_s\text{min}/R_s\text{min}. \qquad \ldots(5)$$

The collector current required to bottom the transistor is increased by R_3 which is effectively in parallel with $R_s + R_g$. The current required for this will be

$$I_{R3}\text{max} = (V_{cc}\text{max} - V_{ce(sat)} - V_{D1})/R_3\text{min}. \qquad \ldots(6)$$

Therefore the maximum collector current requirement (I_c max) is given by

$$I_c\text{max} = \frac{V_s\text{min}}{R_s\text{min}} + \frac{V_{cc}\text{max} - V_{ce(sat)} - V_{D1}}{R_3\text{min}} \qquad \ldots(7)$$

and therefore the base current I_b required is

$$I_b = I_c\text{max}/h_{FE}\text{min}. \qquad \ldots(8)$$

Some of the current supplied by the driving pulse will be taken by the stabilising resistor R_2.

To ensure that the transistor base is normally reverse biased by 0·2V at the maximum working temperature, the criterion for R_2 is

$$R_2 . I_{CBO} + 0{\cdot}2 \leqslant V_{D1}\text{min}$$

so that

$$R_2 = (V_{D1}\text{min} - 0{\cdot}2)/I_{CBO}. \qquad \ldots(9)$$

Drive Current

Assuming that the input to the base is approximately equal to a high value of $r_{bb'}$, then the drive current required is given by

$$I_{in} = I_b(r_{bb'} + R_2)/R_2. \qquad \ldots(10)$$

The voltage required is given by

$$V_{in} = I_{in}\left(R_1 + \frac{R_2 r_{bb'}}{R_2 + r_{bb'}}\right) + V_{be} + V_{D1}. \qquad \ldots(11)$$

Two design examples and practical circuits are given in the Appendix.

MONOSTABLE CIRCUITS

It is sometimes necessary to increase the duration of an existing pulse to make it suitable for triggering an SCR. This is particularly so where inductive loads are used. A suitable circuit to meet this requirement is the monostable circuit.

Circuit Operation

The operation of the monostable circuit using two d.c. supplies is discussed in Refs. 2 and 3. However, a simplified version using only one supply is suitable for triggering SCRs. This is shown in Fig. 2.

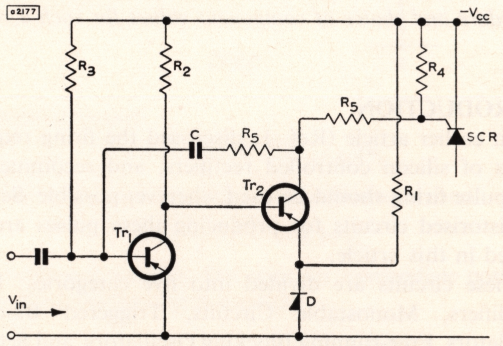


Fig. 2—Monostable circuit

Under steady state conditions, Tr_1 is bottomed and Tr_2 cut off by the voltage across D (normally a silicon diode) exceeding the maximum bottoming voltage of Tr_1. The only current flowing in the collector of Tr_2 is the leakage current I_{CBO}. Capacitor C is charged almost to V_{cc} via R_s, R_5, R_4 and the base-emitter diode of Tr_1.

Application of a trigger pulse to the base of Tr_1, to cut off this transistor, causes the current flowing in R_2 to bottom Tr_2. At the same time, Tr_1 base will be driven positive by the charge on C. This quasi-stable state continues until C has discharged through R_3 and I_{CBO} of Tr_1. The circuit then returns to the stable state. To prevent the SCR triggering on the leakage current of Tr_2, R_4 is introduced and R_5 limits the base current of Tr_1 while C recharges during the recovery period.

Circuit Design

So that the SCR will not be fired by the leakage current of Tr_2, assume that all the leakage current flows through R_4, then

$$R_4 < V_{NF}/I_{CBO}\text{max} \qquad \ldots(12)$$

where V_{NF} = maximum voltage which will not fire the SCR at maximum junction temperature and I_{CBO} max = maximum leakage current in Tr_2.

In practice, some of the leakage current will flow through the SCR gate-cathode junction and the voltage developed will be less than V_{NF}.

The value of $R_s$min may be found from the SCR data in the normal way, remembering that the source voltage is less than V_{cc} by the diode voltage drop and the maximum bottoming voltage of Tr_2.

Ignoring the gate-cathode resistance of the SCR and the resistance of the base-emitter junction of Tr_1, we find that

$$R_5 > \frac{V_{cc}\text{max}}{I_{b1}\text{max} - \dfrac{V_{cc}\text{max}}{R_3\text{min}}} - R_s\text{min} \qquad \ldots(13)$$

where V_{cc}max = maximum applied voltage allowing for tolerance on the supply and I_{b1}max = maximum rated base current of Tr_1.

The maximum dissipation in Tr_2 may now be determined and the transistor selected. We must choose R_1 so that the current through D develops a voltage across D greater than the maximum bottoming voltage of Tr_1.

The maximum value of R_2 may now be found. From the maximum value of I_{c2} and the minimum value of h_{FE} of Tr_2, the minimum base current (I_{b2}min) in Tr_2 may be found, so that this transistor is bottomed during the quasi-stable state.

Hence

$$R_2 < \frac{V_{cc} - (V_D + V_{be}\text{max})}{I_{b2}\text{min} + I_{CBO}\text{max}} \qquad \ldots(14)$$

where V_D = voltage drop across D and V_{be}max = maximum base-emitter voltage for Tr_2 when bottomed.

Consideration may now be given to R_3. Having found R_2, $I_c$max in Tr_1 may be found and so I_{b1}min calculated using the minimum h_{FE} of Tr_1.

Then

$$R_3 < \frac{V_{cc}\text{min} - V_{be}}{I_{b1}\text{min}}. \qquad \ldots(15)$$

R_3 may also be found from a knowledge of I_{b1}max for Tr_1, that is

$$R_3 > \frac{V_{cc}\text{max} - V_{be}}{I_{b1}\text{max}}. \qquad \ldots(16)$$

Selecting a value within this range will depend on the requirements of the circuit. If high temperature (60°C) operation is required with a stable pulse duration, R_3 should be small. Conversely, as long as the pulse duration is sufficient to trigger the SCR, a constant duration with temperature may not be necessary. Hence, greater sensitivity may be obtained with a higher value of R_3. A value giving 10 to 25 times I_{CBO}max in place of I_{b1} is satisfactory for general use.

The value of the feedback capacitor C may be found from a knowledge of R_3 and the required pulse duration.

Generally, $R_5 \ll R_3$, so that the normal expression for pulse duration may be used, that is

$$t \simeq 0{\cdot}7CR_3. \qquad \ldots(17)$$

TRIGGERED BLOCKING OSCILLATORS

Triggered blocking oscillators are useful where a pulse of insufficient duration and power to drive an SCR is available, and it is required to transform this into a pulse suitable for firing the SCR. This circuit will trigger at very low current levels, and provide a suitable output pulse with constant duration. Two versions, for small and large SCRs, are described.

Circuit Operation (1)

In Fig. 3, the transistor is biased off by the potential across the conducting diode D_1. When a negative pulse is applied to the input causing emitter current to flow, then, provided that the loop gain is high enough, the transistor will bottom regeneratively. When the collector current has risen to h_{FE} times the base current, conduction will cease regeneratively. The transistor will then be non-conducting again, and ready to receive the next input pulse. This operation produces a pulse, across winding n_1 of the transformer, which can be applied to the SCR.

Circuit Design (1)

With this circuit the output voltage V_{n1} across n_1 will be greater than V_{cc}. This follows because of the positive voltage developed across n_2. The transistor bottoms and, since the transistor is hard 'on' during the pulse, the base voltage rises almost to the emitter voltage.

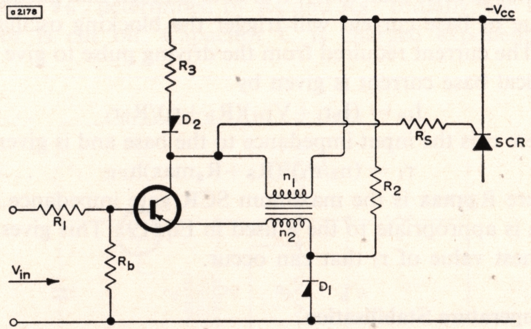


Fig. 3—Triggered blocking oscillator circuit

An approximate expression for V_{n1}, in which transformer losses are ignored, is

$$V_{n1} = \frac{V_{cc} - V_{CE(knee)}}{1 - \dfrac{n_2}{n_1}}. \qquad \ldots(18)$$

The circuit will not regenerate unless $n_1/n_2 > 1$. This can be seen from the loop gain equation (which must be satisfied for regeneration).

$$\frac{R_s\dfrac{n_1}{n_2}}{\left(\dfrac{n_1}{n_2}\right)^2(1-\alpha)\left(\dfrac{25}{I_b} + r_{bb'} + R_b\right) + R_s} > 1 \qquad \ldots(19)$$

where I_b is the transistor base current in mA and $r_{bb'}$ is the internal base resistance of the transistor. This expression can be used to calculate the value of I_b to trigger the circuit.

The pulse duration is determined by the inductance of the transformer winding n_1, and the emitter current I_e which is given by the voltage across the transformer secondary V_{n2} divided by the input resistance to the emitter, r_{1e}. The value of r_{1e} changes during the pulse, however, since it is dependent on α and the value of base resistance used.

The value of r_{1e} required for a given pulse duration is given by the equation

$$r_{ie} = \frac{[1-(n_2/n_1)][V_{n1}(n_2/n_1)-V_{be}]}{V_{n1}/R_S+V_{n1}t/L_{n1}} \qquad \ldots(20)$$

where t = pulse duration required, L_{n1} = primary inductance, and r_{ie} = input impedance of the transistor emitter and is given by the expression

$$r_{ie} = r_e+(r_{bb'}+R_b)(1-\alpha). \qquad \ldots(21)$$

Under the conditions being considered, r_e is very small, and Eq.(21) can be rearranged to give

$$R_b = \frac{r_{ie}}{1-\alpha} - r_{bb'}. \qquad \ldots(22)$$

Pulse Drive Requirements

To find the trigger current required from the driving pulse, Eq.(19) can be used in conjunction with published data. From this data the lowest value of α can be found for different values of collector current. To use Eq.(19), a value of collector current must be taken arbitrarily which gives a value of α and I_b. These values must then be substituted in Eq.(19) when the expression must give a value greater than unity. If it does so, then that particular value of base current will trigger the blocking oscillator.

The current required from the driving pulse to give this critical base current is given by

$$I_{in} = (I_b r_i+V_{D1})(R_b+r_i)/R_b r_i \qquad \ldots(23)$$

where r_i is the input impedance to the base and is given by

$$r_i = (n_2/n_1)^2(R_S+R_g\text{max})h_{FE} \qquad \ldots(24)$$

where R_g max is the maximum SCR gate impedance and h_{FE} is appropriate to the α used in Eq.(19). This gives the highest value of r_i that can occur.

Temperature Stabilisation

The voltage across diode D_1 reverse-biases the base-emitter junction of the transistor, and prevents I_{CEO} from flowing. The current I_{CBO} flows only through R_b, which must not be greater than 1kΩ if this control is to be effective up to 55°C ambient.

Circuit Recovery Time

The recovery time of the circuit is determined by the primary magnetising current of the transformer, I_{n1}, at the end of the pulse, the inductance of the winding, L_{n1}, and the reverse voltage which is permissible at the collector. The value of I_{n1} flowing at the end of the pulse will continue to flow in L_{n1} at the instant the transistor switches off, and the reverse voltage appearing will be determined by the resistance left in the circuit. The value of current in n_1 at the end of the pulse is determined by I_e and I_s.

$$I_e = V_{n2}/r_{ie}. \qquad \ldots(25)$$

As I_e does in fact increase as the collector current increases due to changes in the value of α as the transistor comes out of bottoming, the above expression is approximate.

Then

$$I_{n1\,final} = I_e\text{max}-I_S \qquad \ldots(26)$$

where I_S is the current through R_S and the SCR gate.

To limit the reverse voltage across R_S to the maximum reverse gate voltage rating of the SCR, a diode D_2 and resistance R_3 must be included such that

$$R_3 \leqslant V_{GR}/I_{n1} \qquad \ldots(27)$$

where V_{GR} = SCR maximum reverse gate voltage rating.

The recovery time t_R of the circuit is determined by

$$t_R = 4L_{n1}/R_3. \qquad \ldots(28)$$

It is possible to trigger the circuit before this period has elapsed by increasing the amplitude of the input pulse.

Circuit Operation (2) (Fig. 4)

The transistor is normally non-conducting with its base-emitter junction reverse-biased by the voltage V_{D2} across the diode D_2, which is caused by current through D_2 and R_3. The value of R_2 is chosen so that the collector leakage current does not exceed I_{CBO}.

If a negative pulse is applied to C and current flows through the base, the transistor will bottom because of the positive feedback from n_1 to n_2, and will be held in this condition by the current from winding n_2. This current, I_b, is constant during the pulse, while the collector current increases owing to the inductance of n_1. When the collector current reaches a value of $h_{FE}I_b$, the transistor will cease to conduct regeneratively and will then be ready for the next incoming pulse. During this time a positive-going pulse is applied via R_s to the SCR.

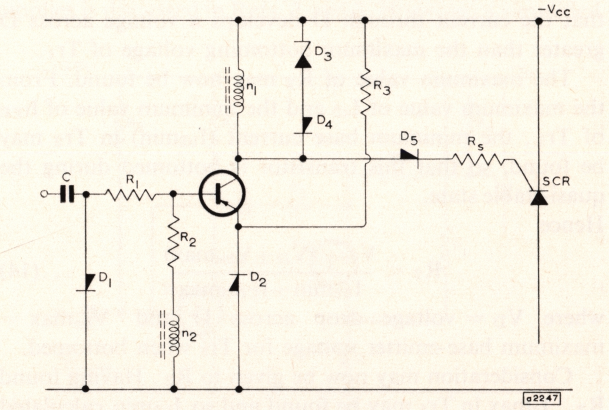


Fig. 4—Triggered blocking oscillator for use with large SCRs

Circuit Design (2)

The maximum initial available voltage across the collector winding, V_{n1}max, is given by

$$V_{n1}\text{max} = V_{cc}\text{max}-V_{D2} \qquad \ldots(29)$$

where V_{D2} is the voltage drop across diode D_2.

The minimum initial voltage available across the collector winding, V_{n1}min, is given by

$$V_{n1}\text{min} = V_{cc}\text{min}-V_{ce(sat)}-V_{D2}. \qquad \ldots(30)$$

If we choose a value between these two limits, we can find a source voltage, V_s, for firing the SCR. From the firing circuit design curves (Ref. 1) the appropriate value of source resistance, R_s, can be found.

For temperature stability R_2 must not be greater than a value determined by the leakage current, I_{CBO}, at the maximum ambient temperature, that is

$$I_{CBO}R_2 \leqslant V_{D2}\text{min}-0{\cdot}2.$$

Therefore

$$R_2 \leqslant (V_{D2}\text{min}-0{\cdot}2)/I_{CBO}. \qquad \ldots(31)$$

This ensures that the base-emitter junction of the transistor is always reverse-biased by at least 0·2V at the maximum ambient temperature.

The final current flowing in the collector winding is given by

$$I_{n1(final)} = V_{cc}t_p/L_{n1} \qquad \ldots(32)$$

where t_p is the duration of the output pulse, and L_{n1} is the inductance of the collector winding.

The magnetising force in the coil, H (oersteds), is given by

$$H = (4\pi n_1 I_{n1(final)})/10\ell \qquad \ldots(33)$$

where n_1 is the number of turns in the collector winding and ℓ is the length of the magnetic path in the core (in centimetres).

If the design is such that the value of H is sufficiently high to drive the core into saturation, the output pulse duration will be almost independent of h_{FE}, as, once saturation has been reached, increasing magnetising current will not appreciably increase the pulse duration.

From Eq.(33), n_1 can be found by setting a limit on the value of $I_{n1(final)}$, choosing a particular core type and consulting the Ferroxcube data and choosing a value of H such that the core is saturated.

From this value of n_1, the value of L_{n1} can be found for the particular core type used, and from Eq.(32) t_p can then be found.

The final collector current, I_c, is given by

$$I_c = \frac{V_{cc}\text{max}-V_{ce(sat)}-V_{D2}}{R_s\text{min}} + \\ + \frac{V_{cc}\text{max}-V_{ce(sat)}-V_{D2}}{N^2R_2\text{min}} + I_{n1(final)} \qquad \ldots(34)$$

where N is the transformer turns ratio, that is, n_1/n_2.

The base current required, I_b, is given by

$$I_b = I_c/h_{FE}\text{min}. \qquad \ldots(35)$$

The voltage required across n_2, V_{n2}, is given by

$$V_{n2} = I_b \times R_2. \qquad \ldots(36)$$

The resistance of the transformer winding can be neglected compared with R_2, hence

$$N = n_1/n_2 = V_{n1}/V_{n2} = V_s/V_{n2}. \qquad \ldots(37)$$

From Eqs.(35), (36) and (37)

$$n_1/n_2 = V_s h_{FE}\text{min}/R_2I_c. \qquad \ldots(38)$$

From Eqs.(34) and (38)

$$\frac{(V_{cc}\text{max}-V_{ce(sat)}-V_{D2})N^2}{R_s\text{min}} + I_{n1(final)}N^2 - \\ - \frac{V_s h_{FE}\text{min}}{R_2}.N + \frac{(V_{cc}\text{max}-V_{ce(sat)}-V_{D2}}{R_2\text{min}} = 0. \qquad \ldots(39)$$

This is a quadratic equation in N, and hence a suitable value of N can be found.

Pulse Drive Requirements

There is a voltage drop of $(V_{be}+V_{D2})$ between the base of the transistor and ground. Therefore the amplitude of the pulse must be sufficient to overcome this voltage drop. If this amplitude is V_1, and if V_2 is the voltage to which C can discharge, then C is given by

$$C = \frac{t}{R_1 \log_e \frac{V_1}{V_2}} \qquad \ldots(40)$$

where t is the effective duration of the input pulse.

Regeneration

For regeneration the equation

$$(R_s h_{FE} N)/(N^2R_2+R_s) \geqslant 1 \qquad \ldots(41)$$

must be satisfied. In the limit

$$h_{FE(lim)} = (N^2R_2+R_s)/R_sN. \qquad \ldots(42)$$

The value of collector current at this value of h_{FE} can be found from the data sheets for the transistor used. This is the minimum value of collector current at which the circuit will regenerate. Dividing this value by $h_{FE(lim)}$ gives the base current required to trigger the blocking oscillator.

FREE-RUNNING BLOCKING OSCILLATORS

The blocking oscillator shown in Fig. 5 (Ref. 4) is a free-running circuit, and provides a train of firing pulses of known amplitude and frequency. This circuit is suitable for firing a single SCR used in an inverter or chopper application.

Circuit Operation

The base of the transistor in Fig. 5 is at a positive potential, V_b, determined by R_2 and R_3. Initially, the transistor is cut off. Capacitor C is charged exponentially through R_1 (and transistor leakage current, if appreciable) to the supply voltage. When the voltage across the capacitor exceeds the bias voltage at the base by an amount sufficient to cause the transistor to conduct, the blocking oscillator will bottom by regenerative action.

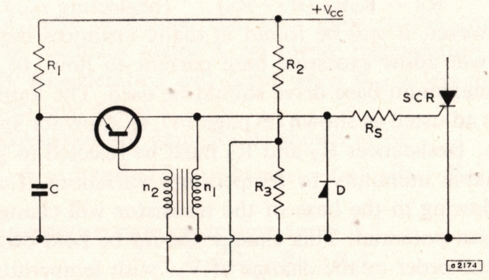


Fig. 5—Free-running blocking oscillator

The transistor continues to conduct while C is discharging through the transistor, until the capacitor voltage has fallen to a value V_c, where

$$V_c = V_b/[1+(n_2/n_1)].$$

During this period a pulse is applied to the SCR gate through series resistance R_S. As before, the capacitor then starts to charge until the blocking oscillator regenerates again. Diode D limits the reverse voltage across the SCR gate-cathode junction.

The 'off' period of this circuit is determined by the values of R_1 and C. The pulse duration is determined approximately by the values of C, R_s, and the SCR gate impedance.

Circuit Design

From the SCR firing circuit design curves (Ref. 1) the required output pulse amplitude can be found, using the

50% duty cycle curves. From the tolerances quoted, maximum and minimum values can be deduced.

Since the pulse from this circuit is derived from a capacitor C, the initial value V_b must not exceed $V_s$max; and after the required time t the pulse must not have fallen below V_s min. The pulse may continue beyond time t, with an exponentially falling output less than $V_s$min, and this output cannot be relied upon for firing the SCR.

The value of capacitor required is given by

$$C_1 = \frac{t}{\dfrac{(R_s+R_g)(n_1/n_2)^2R_b}{(R_s+R_g)+(n_1/n_2)^2R_b}\log_e\dfrac{V_b}{V_s\text{min}}}. \quad \ldots(43)$$

In this equation the time constant will vary with a change of SCR because of variations of R_g. However, when a low value of R_g gives a small time constant, $V_s$min will also be small, and these two effects tend to cancel, so that the expression for C_1 can be simplified. If R_g is a minimum, then

$$C_1 = \frac{t}{R_s\log_e(V_b/V_s\text{min})}. \quad \ldots(44)$$

It can be shown that the transformer ratio to give maximum loop gain is given by

$$n_1/n_2 = (R_s/R_b)^{\frac{1}{2}}$$

where

$$R_b = R_2R_3/(R_2+R_3) \qquad \text{(neglecting } r_{bb'}\text{)}.$$

However, it will be found in many instances that this value will allow excessive base current to flow. In these cases maximum base drive should be used. The loop gain can be adjusted as shown on page 147, to allow for spreads in h_{FE}. Resistances R_2 and R_3 must be selected to give a reasonable immunity to temperature variations. Current I_{CBO} flowing in the base of the transistor will change the base bias potential. This change should be held down to the same order as the change of V_{be} with temperature.

Applying this criterion

$$I_{CBO}\text{max}[R_2R_3/(R_2+R_3)] \leqslant 0{\cdot}2\text{V}. \quad \ldots(45)$$

Also

$$V_b = V_{cc}R_3/(R_2+R_3). \quad \ldots(46)$$

The actual value of base bias voltage should be high enough to reduce the effect of V_{be} changing with temperature. From Eqs.(45) and (46), values for R_2 and R_3 can be calculated.

Transformer Design

To calculate the required transformer ratio, suppose the voltage across n_1 at the moment of switching on is such as to produce a base current equal to the maximum rating. If $r_{bb'}$ is ignored (a safe procedure, since $r_{bb'}$ would reduce I_b) the base current is given by

$$I_b = V_b(n_2/n_1)/R_b$$

where

$$R_b = (R_2R_3)/(R_2+R_3).$$

Thus

$$n_2/n_1 = (I_bR_b)/V_b. \quad \ldots(47)$$

The capacitor will now discharge to a voltage V_c given by

$$V_c = \frac{V_b}{1+(n_2/n_1)}. \quad \ldots(48)$$

For the blocking oscillator to behave as a d.c. switch, its own natural period must be longer than the time taken for the capacitor to reach the voltage V_c given by the above equation. The natural period t_n of the blocking oscillator with transformer primary inductance L_{n1} is

$$t_n = \frac{L_{n1}h_{FE}R_s(n_1/n_2)-(n_1/n_2)^2R_b-R_s}{(n_1/n_2)^2R_bR_s}. \quad \ldots(49)$$

The time t_p taken for the capacitor to reach V_c is given by

$$t_p = \frac{C(R_g+R_s)R_b(n_1/n_2)^2}{R_g+R_s+R_b(n_1/n_2)^2}\log_e(V_b/V_c). \quad \ldots(50)$$

Thus when $t_n > t_p$, the period will be determined by Eq.(50).

The calculation of the transformer inductance can be simplified by assuming that the capacitor voltage is constant.

The inital current I_{n1} in n_1 is given by

$$I_{n1} = V_b(n_2/n_1)^2/R_b. \quad \ldots(51)$$

If the magnetising current at the end of the period t_p is designed to be $0{\cdot}5I_{n1}$, then the primary inductance L_{n1} of the transformer is given by

$$L_{n1} \geqslant V_bt_p/0{\cdot}5I_{n1}. \quad \ldots(52)$$

With inductance calculated by this method, the pulse duration is made independent of transistor gain variations.

Maximum Value of R_1

If R_1 is made larger than a certain value, the circuit will cease to oscillate. This is due to variations of α with emitter current. The value of emitter current I_e at which this occurs is given by

$$I_e = (V_{cc}-V_b)/R_1. \quad \ldots(53)$$

It is possible to determine whether the circuit will be regenerative for a given value of R_1.

The h_{FE} required for regeneration is given by

$$h_{FE} \geqslant \frac{(n_1/n_2)^2(R_b+r_{bb'})+R_s}{[(n_1/n_2)I_eR_s-25(n_1/n_2)]/I_e} \quad \ldots(54)$$

where I_e is in mA.

Since the value of collector current is nearly the same as the emitter current, the current value can be obtained from Eq.(51).

Eq.(54) must give h_{FE} less than or equal to that given in published data.

The time for C to recharge from V_c to V_b is given by

$$t_{charge} \simeq CR_1\log_e\left(\frac{V_{cc}-V_c}{V_{cc}-V_b}\right). \quad \ldots(55)$$

SCHMITT CIRCUITS

The circuit shown in Fig. 6 is suitable for applications where the trigger level is required to be predictable, but where the level at which the gate signal is removed may be undefined. This circuit would be suitable for any application where it is required to switch on the SCR when a specific voltage is reached on a sawtooth input signal. It is particularly suitable for phase control circuits where it is required to maintain the gate firing voltage to the end of the conducting period. A more complex circuit which turns 'on' and 'off' at defined levels is described on page 148.

Circuit Operation

It is convenient to refer the input signal to the same common line as the SCR cathode. When the input voltage is zero, Tr_1 will be fully conducting and bottomed, and Tr_2 will be held non-conducting, and in fact reverse-biased, by the resistors R_2 and R_3.

If a positive-going signal is supplied through a source resistance R_{ss} such that the signal can be regarded as a voltage source, then the emitter voltage V_e will follow this signal, and consequently the collector current of Tr_1 will become less, making the base voltage V_{b2} of Tr_2 negative. When V_{b2} is slightly more negative than V_e, and provided that there is sufficient loop gain in the circuit, Tr_1 will cease to conduct and Tr_2 will bottom, this action being regenerative.

Since the spreads of SCR gate impedance R_g are so great, it must be arranged that Tr_2 will bottom when R_g is a minimum, so that in practice the degree of bottoming of Tr_2 is not known. Because of this, the input voltage level at which the circuit will regeneratively remove the SCR gate signal is not definable.

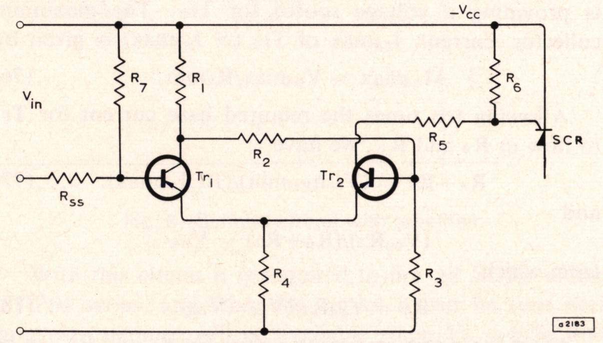


Fig. 6—Basic Schmitt circuit

If there is a possibility that the input may be accidentally open-circuited, a resistor R_7 which will provide enough base current to bottom Tr_1 should be connected between the base of Tr_1 and the negative line.

Circuit Design

The design must be based on the minimum value of R_g—that is, it is assumed to be a short circuit. Thus, since Tr_2 will bottom, the effective SCR firing source voltage V_s is given by

$$V_s \simeq V_{cc}-V_{ce(sat)} \quad \ldots(56)$$

and the effective source resistance R_s is given by

$$R_s \simeq R_4+R_5. \quad \ldots(57)$$

Thus the maximum value of collector current I_{c2} in Tr_2 is

$$I_{c2}\text{max} = (V_{cc}-V_{ce(sat)})/(R_4+R_5) \quad \ldots(58)$$

and hence the maximum base current I_{b2} of Tr_2 is

$$I_{b2}\text{max} = [V_{cc}-V_{ce(sat)}]/[(R_4+R_5)h_{FE}\text{min}]. \quad \ldots(59)$$

It has been found satisfactory to make the current I_{R1R2R3} in the potentiometer chain of R_1, R_2 and R_3 ten times I_{b2} max, and so

$$I_{R1R2R3} = [10(V_{cc}-V_{ce(sat)})]/[(R_4+R_5)h_{FE}\text{min}] \quad \ldots(60)$$

and

$$R_1+R_2+R_3 = V_{cc}/I_{R1R2R3}. \quad \ldots(61)$$

It must be arranged that when Tr_1 is bottomed, the base-emitter junction of Tr_1 is reverse-biased. The circuit will then be regenerative.

From the known value of V_e under these conditions, it is now possible to calculate R_3. Thus

$$R_3 = (V_e+V_{be})/I_{R1R2R3} \quad \ldots(62)$$

and, similarly,

$$R_4 = V_e/I_{c2}\text{max}. \quad \ldots(63)$$

The value of R_5 can then be found from Eq.(57).

If the required input trigger voltage V_{on} to make Tr_2 conduct is known, it is possible to calculate the value of R_1 to achieve this. Thus

$$V_{on} = V_{cc}R_3R_4/[R_4(R_1+R_2+R_3)+R_1R_3] \quad \ldots(64)$$

from which

$$R_1 = [V_{cc}R_3R_4-R_4(R_1+R_2+R_3)V_{on}]/V_{on}R_3. \quad \ldots(65)$$

It is now possible to find R_2, since

$$R_2 = (R_1+R_2+R_3)-(R_1+R_3). \quad \ldots(66)$$

To obtain the calculated firing voltage V_{on}, it is necessary to make the source resistance of the signal R_{ss} less than a certain value. It has been found sufficient in practice to make R_{ss} one tenth of the input impedance when Tr_1 is not bottomed. Hence

$$R_{ss} = (h_{FE}\text{min}R_4)/10. \quad \ldots(67)$$

We must determine the loop gain of the circuit A and the feedback factor β, to ensure regeneration of the circuit. Regeneration will occur when R_{ss} is less than the value to give $A\beta = 1$.

The expression for gain can be shown to be

$$A = h_{FE}R_3/[2r_{bb'}+h_{FE}(r_{e1}+r_{e2})+R_{ss}+R_3] \quad \ldots(68)$$

and an approximate expression for β is

$$\beta = R_1/(R_1+R_2+R_3) \quad \ldots(69)$$

where it is assumed that R_3 is small compared with the input impedance to Tr_2 when both transistors are in class A operation at the instant of switching.

To ensure that a circuit will always regenerate, the minimum value of h_{FE} and the maximum value of $r_{bb'}$ must be used. The value of r_e is specific and is given by $(25/I_e)$, where I_e is in mA. Thus, knowing β from circuit values it is possible to specify a value of A to give regeneration. Then from Eq.(68)

$$R_{ss}\text{max} = \{h_{FE}R_3-A[2r_{bb'}+h_{FE}(r_{e1}+r_{e2})+R_3]\}/A \quad \ldots(70)$$

This equation is influenced by the approximation for β (Eq.69) so that the value of R_{ss}max obtained is lower than will be found necessary in practice. In most circuits the value of R_{ss} calculated from Eq.(67) will be quite adequate for regeneration. When considering the case where Tr_2 is only just bottomed, the input signal level V_{off} at which Tr_2 becomes non-conducting is required, and is approximately equal to V_e when Tr_2 is conducting.

It has been found that as the difference between V_{on} and V_{off} is increased, the loop gain is increased, and the permissible value of R_{ss}max is higher. In terms of the design procedure given above, this means that when the value of V_{on} is obtained by selection of R_1, then the higher the value of V_{on} the lower will be the value of A. Consequently R_{ss}max will be smaller.

It is important to include resistor R_6 which prevents

firing of the SCR by the leakage current of Tr_2.
Thus

$$R_6 \leqslant V_{NF}/(I_{CBO}\text{max}) \qquad \ldots(71)$$

where V_{NF} is the maximum gate voltage at which no SCR will fire, at the maximum junction temperature.

Variant of Basic Circuit (Schmitt circuit with specific backlash)

The circuit of Fig. 7 is a modification of the Schmitt trigger circuit of Fig. 6, and is suitable for applications where the 'on' and 'off' trigger levels must be different and precise.

An example of this would be in a temperature controller. Switching off the SCR would be achieved by the anode supply voltage being reduced to zero at a frequency considerably greater than the signal frequency. An unsmoothed rectified mains voltage is suitable as the supply.

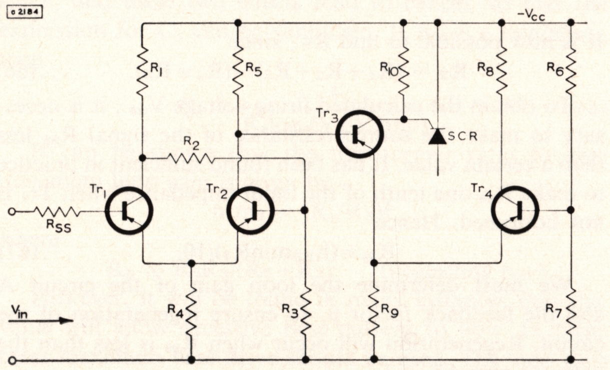


Fig. 7—Schmitt circuit with specific backlash

Transistor Tr_1 is normally held non-conducting by the collector current of Tr_2, which produces a negative voltage V_e across R_4. If the base voltage of Tr_1 is now raised to a value slightly more negative than V_e then, provided that the loop gain is sufficient, the circuit will regenerate to a condition with Tr_1 conducting and Tr_2 non-conducting.

The output from the Schmitt circuit is taken from the collector of Tr_2 and fed into Tr_3, an amplifier stage. Transistor Tr_4 provides a stable emitter voltage (V_3) for Tr_3 so that when Tr_2 is conducting, Tr_3 is biased off.

When Tr_3 conducts, the circuit operation will depend on the value of SCR gate impedance R_g. If R_g is a minimum, the emitter voltage of Tr_4 will rise to near V_{cc} and Tr_4 is cut off. When this happens the SCR is effectively being driven by V_{cc} through R_9 in the normal way, so that R_9 and V_{cc} can be determined from the SCR design curves.

If R_g is at the maximum value, then when Tr_3 is conducting, Tr_4 will be conducting also, and the emitter of Tr_4 will be held at a voltage determined by R_6 and R_7. In this case there is effectively no resistance in series with the SCR, and the voltage applied is $V_{cc}-V_{e3}$, where V_{e3} is the emitter voltage of Tr_3. This voltage must be selected to fire all SCRs without exceeding their ratings.

Having decided on the value of V_{cc}, and knowing the voltage $V_{CE(sat)3}$ across Tr_3, we can then find the value of R_9 from the SCR published data.

The base voltage V_{b4} of Tr_4 must be as high as possible, the limit being set by the SCR voltage drive such that

$$V_{b4}\text{max} = V_{cc}-(V_1+V_{CE(sat)3}) \qquad \ldots(72)$$

where V_1 is the minimum voltage to fire an SCR, and $V_{CE(sat)3}$ is the bottoming voltage of Tr_3.

The maximum collector current I_{c3} in Tr_3 occurs when the SCR gate impedance is a minimum. For design simplicity this is considered as a short circuit, giving

$$I_{c3} = V_{cc}-V_{CE(sat)3}/R_9\text{min}. \qquad \ldots(73)$$

The product $I_{c3}V_{CE3}$ must not exceed the transistor power rating.

The base current required by Tr_3 is given by

$$I_{b3} = I_{c3}\,\text{max}/h_{FE}\text{min}. \qquad \ldots(74)$$

The value of R_5 is given by

$$R_5\text{max} = [(V_{cc}-V_{e3})-V_{be}\text{max}]/I_{b3}\text{max}. \qquad \ldots(75)$$

Transistor Tr_4 must be just clear of bottoming when it is providing a voltage source for Tr_3. The maximum collector current $I_{c4}\text{max}$ of Tr_4 ($\simeq I_{e4}\text{max}$) is given by

$$I_{c4}\text{max} = V_{b4}\text{max}/R_9\text{min}. \qquad \ldots(76)$$

Allowing ten times the required base current for Tr_4 to flow in R_6 and R_7, we have

$$R_6+R_7 = (V_{cc}h_{FE}\text{min})/(10.I_{c4}\text{max}) \qquad \ldots(77)$$

and

$$(V_{cc}R_7)/(R_6+R_7) = V_{b4'}$$

from which

$$R_7 = V_{b4}R_6/(V_{cc}-V_{b4}). \qquad \ldots(78)$$

From these two equations, values for R_6 and R_7 can be calculated. The value of R_8 is obtained from

$$R_8\,\text{max} = [V_{cc}-(V_{b4}+1)]/I_{c4}\text{max}. \qquad \ldots(79)$$

By allowing 1V for V_{cb} in the above equation, we ensure that Tr_4 is never bottomed.

When Tr_2 is conducting, its collector voltage V_{c2} must be a little lower than V_{b4} even when component tolerances are such that the collector voltage in Tr_2 is at a maximum. When tolerances are such that Tr_2 is conducting most heavily, the transistor should be just bottomed. This will maintain the accuracy of the input trigger level.

We must allow for the maximum variation of Schmitt emitter voltage. The limits are:

(i) The maximum must make V_{c2} always below the base voltage of Tr_4.

(ii) The minimum must still be sufficient to swamp any changes in V_{be}.

With an emitter voltage variation from $V_e\text{min}$ to $V_e\text{max}$, there is a corresponding variation of V_{c2} from $V_{c2}\text{max}$ to $V_{c2}\text{min}$.
Then

$$I_{e2}\text{max} = (V_{cc}-V_{c2}\text{min})/R_5\text{max} \qquad \ldots(80)$$

and

$$I_{e2}\text{min} = (V_{cc}-V_{c2}\text{max})/R_5\text{min} \qquad \ldots(81)$$

The permissible extremes of R_4 are given by

$$R_4\text{max} = V_e\text{min}/I_{e2}\text{min} \qquad \ldots(82)$$

and

$$R_4\text{min} = V_e\text{max}/I_{e2}\text{max}. \qquad \ldots(83)$$

The design procedure from this point is the same as for the circuit of Fig. 6, as described on page 147.

Circuit Design (Schmitt circuit with amplifier)

Since the Schmitt may remain in a condition of sustained output the design must be based on SCR gate dissipation under d.c. conditions, that is 100% duty cycle.

The required SCR firing conditions can be seen from the curves in Ref. 1. It can be seen from the curves that it is desirable to work at the values of V_s and R_s that give the greatest tolerance in V_s.

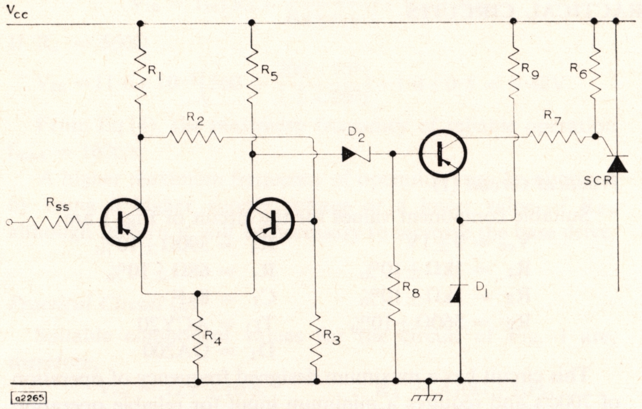


Fig. 8—Schmitt circuit with amplifier

With this circuit it is required to fire all SCRs of the BTY64 series, and from the curves it can be seen that greatest tolerance will be available when $V_s = 6{\cdot}5$V and $R_s = 22\Omega$.

The Schmitt circuit with amplifier is shown in Fig. 8. The function of R_6 is two-fold: (i) with a supply voltage of 12V, it enables the effective value of V_s to be chosen for maximum tolerance, and (ii) it prevents the leakage current of Tr_3 firing the SCR. This latter criterion can be seen from the expression

$$R_6 \leqslant V_{NF}/I_{CBO}\text{max}. \qquad \ldots(84)$$

For given values of V_{cc}, V_s and R_s the required values of R_6 and R_7 can be calculated.

If we consider a low-impedance SCR gate as a short circuit across R_6, then the short-circuit current required from Tr_3 is given by

$$\frac{V_{cc}-V_{D1}-V_{ce\,sat}}{R_s} = \frac{V_s}{R_s}$$

and

$$R_7 = R_s(V_{cc}-V_{D1}-V_{ce\,sat})/V_s \qquad \ldots(85)$$

where V_{D1} is the forward drop across diode D_1. A value of R_6 must now be selected to give the required open-circuit gate voltage, V_s. Thus

$$(V_{cc}-V_{D1}-V_{ce\,sat})R_6/(R_6+R_7) = V_s.$$

Therefore

$$R_6 = V_sR_7/(V_{cc}-V_{D1}-V_{ce\,sat}-V_s). \qquad \ldots(86)$$

The maximum collector current (I_{c3}) required from Tr_3 is given by

$$I_{c3}\text{max} = (V_{cc}-V_{D1}\text{min}-V_{ce\,sat}\text{min})/R_7 \qquad \ldots(87)$$

and the base current I_{b3} required by Tr_3 is given by

$$I_{b3} = I_{c3}\,\text{min}/h_{FE}\text{min}.$$

R_8 is a temperature stabilising resistor for Tr_3. Its value is calculated from Eq.(9).

$$R_8 \leqslant (V_{D1}\text{min}-0{\cdot}2)/I_{CBO}\text{max}. \qquad \ldots(88)$$

It must now be arranged that when Tr_3 is conducting, its collector voltage V_{ce} is about 0·5V below the zener voltage of the zener diode.

The value of R_5 required, ignoring the effect of V_{be}, is given by

$$R_5 = \frac{(V_{cc}-V_z\text{max})R_8\text{min}-I_{b3}R_8\text{min}\,r_{bb'}}{I_{b3}(R_8\text{min}+r_{bb'})} \qquad \ldots(89)$$

If the emitter voltage of T_{r3} when conducting is known, the Schmitt circuit can be designed in the way described on page 147.

REFERENCES

1. JARRATT, T. J. 'Firing Requirements for Silicon Controlled Rectifiers'. **Mullard Technical Communications.** Vol. 6, No. 55, March 1962, pp. 216 to 231.
2. WOLFENDALE, E. (Editor). 'The Junction Transistor and its Applications'. Heywood and Co. Ltd., 1958.
3. 'Reference Manual of Transistor Circuits'. Mullard Ltd. Second edition, 1961.

Design examples and practical circuits are given on pages 150 to 157

APPENDIX

DESIGN EXAMPLES AND PRACTICAL CIRCUITS

Pulse Amplifier Firing Circuits (Fig. 1)

Design Example (1)

Given a supply voltage of 9V with a tolerance of ±1V, it is required to fire a BTZ18 type SCR with a pulse of 50µs at ambient temperatures up to 55°C.

For design purposes take $I_{CBO} = 0{\cdot}25$mA at $T_j = 75$°C for an ACY20 transistor. Then if $R_3 = 560\Omega\pm10\%$, from Eq.(1), $V_p = 8-0{\cdot}4-1{\cdot}0-0{\cdot}14 = 6{\cdot}4$V.

To allow for the exponential fall of the pulse, and for the reduction of V_p at higher frequencies, design for a minimum pulse amplitude of 4·5V, that is, $V_s\text{min} = 4{\cdot}5$V.

It can be seen that the maximum pulse amplitude that can occur is $(V_{cc}\text{max}-V_{D1})$, therefore

$$V_s\text{max} = 9{\cdot}5\text{V}.$$

For the SCR types considered, $V_1=2$V and $i_1=30$mA, thus $R_s\text{ max}=(4{\cdot}5\text{V}-2\text{V})/30\text{mA}=83\Omega$. Let $R_s=68\Omega\pm10\%$.

It can be seen from the firing curves for 50% duty cycle that if $R_s = 68\Omega\pm10\%$, then $V_s = 9{\cdot}5$V. There is a tolerance on this of ±52%. With these values a variation of V_s from 4·5V to 14·5V is permissible, which is more than adequate for this case.

The value of C_1 can now be calculated from Eq.(2)

$$C_1 = \frac{50\times10^{-6}}{61\times0{\cdot}095} = 8{\cdot}6\mu\text{F}.$$

A value of 8µF is suitable.
The maximum value of collector current can be found from Eq.(7).

$$I_c\text{max} = \frac{4{\cdot}5\text{V}}{61} + \frac{10-0{\cdot}5-0{\cdot}5}{500} = 92\text{mA}.$$

With an ACY20 transistor, a minimum h_{FE} of 30 can be taken for design purposes. Thus I_b can be calculated from Eq.(8):

$$I_b = 92\text{mA}/30 = 3{\cdot}1\text{mA}.$$

The value of R_2 can be calculated from Eq.(9):

$$R_s(0{\cdot}5-0{\cdot}2)/0{\cdot}25\text{mA} = 1{\cdot}2\text{k}\Omega.$$

Thus let $R_2 = 1\text{k}\Omega\pm10\%$.

The diode D_1 (OA200) should be operating at about 20mA to give the required forward voltage drop.

$$\text{Thus}\quad R_4 \simeq 7\text{V}/20\text{mA} = 350\Omega.$$
$$\text{Hence let}\quad R_4 = 390\Omega\pm10\%.$$

For a maximum $r_{bb'}$ of 200Ω, the current required from the input pulse I_{in} can be obtained from Eq.(10):

$$I_{in} = \frac{3{\cdot}1\times10^{-3}\times1200}{1000} = 3{\cdot}7\text{mA}.$$

Similarly, if R_1 is 1kΩ the voltage required, V_{in}, can be calculated from Eq. (11).

$$V_{in} = 3{\cdot}7\times10^{-3}\left(10^3+\frac{10^3\times200}{1{\cdot}2\times10^3}\right) + 1{\cdot}5 = 5{\cdot}7\text{V}.$$

The maximum frequency of reliable operation (f_{max}) can be calculated from Eq.(4). This gives

$$f\text{max} = 700\text{c/s}.$$

Practical Circuit (1)

Suitable component values for the circuit of Fig. 1 are:

$V_{cc} = 9\pm1$V $\qquad R_4 = 390\Omega\pm10\%$
$R_1 = 1\text{k}\Omega\pm10\%$ $\qquad R_s = 68\Omega\pm10\%$
$R_2 = 1\text{k}\Omega\pm10\%$ $\qquad C_1 = 8\mu$F
$R_3 = 560\Omega\pm10\%$ $\qquad Tr_1 = $ ACY20
$D_1 = $ OA200

This circuit has a maximum designed frequency of operation of 700c/s and requires a minimum input for reliable operation of 5·7V and 3·7mA.

Design Example (2)

With a supply voltage of 12V±10% it is required to fire a BTY64 with a pulse of 50µs at ambient temperatures up to 55°C.

For design purposes, take $I_{CBO} = 0{\cdot}25$mA for an ACY20 transistor with $T_j = 75$°C.
Eq.(1) gives

$$V_p = V_{cc}\text{min}-V_{ce(sat)}-V_{D1}-I_{CBO}R_3.$$

Then if $R_3 = 560\Omega\pm10\%$

$$V_p = 10{\cdot}8-0{\cdot}4-1{\cdot}0-0{\cdot}14 = 9{\cdot}2\text{V}.$$

To allow for the exponential fall of the pulse, and for the reduction of V_p at higher frequencies, design for a minimum pulse amplitude of 8·0V.
That is $V_s\text{min} = 8{\cdot}0$V.

It can be seen that the maximum pulse amplitude that can occur is $V_{cc}\text{max}-V_{D1}$, therefore $V_s\text{max} = 13{\cdot}2-0{\cdot}5 = 12{\cdot}7$V. For the SCR type considered, $V_1 = 3$V and $i_1 = 130$mA, therefore

$$R_s\text{ max} = (V_s\text{min}-V_1)/i_1 = 38\Omega \quad (\text{Eq.(3)}).$$

Thus take $R_s = 33\Omega\pm10\%$.

The permissible tolerance of V_s may be found from

$$\begin{aligned}V_s\text{min} &= i_1R_s\text{max}+V_1\\ &= 130\times10^{-3}\times36{\cdot}3+3{\cdot}0\\ &= 7{\cdot}7\text{V}\end{aligned}$$

and $V_s\text{max}=[V_g\text{ max }(R_s\text{min}+R_g\text{max})]/R_g\text{max} = 12{\cdot}9$V.
This gives a tolerance of V_s from 7·7 to 12·9V, and thus the practical range of V_s is permissible.

Eq.(7) gives the maximum value of collector current,

$$I_c\text{max} = V_s\text{min}/R_s\text{min}+(V_{cc}\text{max}-V_{ce(sat)}-V_{D1})/R_3\text{min} = 292\text{mA}.$$

The base current I_b is given by,

$$I_b = \frac{I_c\text{max}}{h_{FE}\text{min}} \quad (\text{Eq.(8)})$$

With an ACY20 transistor a minimum h_{FE} of 30 can be assumed, therefore

$$I_b = 292/30 = 9{\cdot}7\text{mA}.$$

R_2 is given by $R_2 \leqslant (V_{D1}\text{min}-0{\cdot}2)/I_{CBO} = 1{\cdot}2\text{k}\Omega$. (Eq.(9)).
Thus take $R_2 = 1{\cdot}0\text{k}\Omega\pm10\%$.

The diode D_1 (OA200) should be operating at about 20mA to give the required forward voltage drop, therefore

$$R_4 = (V_{cc}\text{min}-V_{ce(sat)}-V_{D1})/20 = 490\Omega.$$

Hence take $R_4 = 470\Omega\pm10\%$.

The current I_{in} required from the input pulse can be obtained from Eq.(10).

$$I_{in} = \frac{I_b(r_{bb'}+R_2)}{R_2}$$

For a maximum $r_{bb'}$ of 200Ω,

$$I_{in} = 9{\cdot}7\times10^{-3}\times1200/1000 = 11{\cdot}6\text{mA}.$$

Similarly, from Eq.(11)

$$V_{in} = I_{in}\left(R_1+\frac{R_2r_{bb'}}{R_2+r_{bb'}}\right)+V_{be}+V_{D1}.$$

If $R_1 = 560\Omega$

$$V_{in} =11{\cdot}6\times10^{-3}\left(560 + \frac{200\times10^3}{1{\cdot}2\times10^3}\right)+1{\cdot}0+0{\cdot}5 = 9{\cdot}48\text{V}.$$

From Eq.(4), the maximum frequency of reliable operation $f_{max} = 160$c/s.

A higher maximum frequency of operation may be obtained by using a higher supply voltage or a lower value of R_3, although in turn it will be necessary to increase the base drive.

Practical Circuit (2)

Suitable component values for the circuit of Fig. 1 are, therefore,

$V_{cc} = 12\text{V}\pm10\%$ $\qquad R_4 = 470\Omega\pm10\%$
$R_1 = 560\Omega\pm10\%$ $\qquad R_s = 33\Omega\pm10\%$
$R_2 = 1\text{k}\Omega\pm10\%$ $\qquad C_1 = 16\mu$F
$R_3 = 560\Omega\pm10\%$ $\qquad Tr_1 = $ ACY20
$D_1 = $ OA200

This circuit has a maximum designed frequency of operation of 160c/s, and requires a minimum input, for reliable operation, of 10·0V, 11·6mA.

Monostable Circuits (Fig. 2)

Design Example (1)

Given a supply voltage of 12±1V it is required to produce a 2ms pulse to fire a BTZ18 type SCR at ambient temperatures up to 60°C.

Assume the diode voltage drop for the current which flows when Tr_2 is bottomed, plus the bottoming voltage of Tr_2, to be 1·5V.
Hence $V_s = 12-1{\cdot}5 = 10{\cdot}5$V,
$R_s = 120\Omega\pm10\%$ (from the 100% duty cycle curve in Ref. 1).

Therefore, $I_c$max in Tr_2 will be less than 100mA and the maximum dissipation in Tr_2 will be less than 50mW (for a maximum bottoming voltage of 0·5V). Hence, ACY20 transistors may be used.

In addition, V_D must be greater than 0·5V. With an OA200 diode, a current of 10mA will give $V_D > 0{\cdot}5$V and so $R_1 = 1\text{k}\Omega\pm10\%$. The maximum current through D is therefore 110mA and is within the 60°C rating of the OA200.

At 50mW, and with no heatsink, $\theta_{j-a} = 0{\cdot}25$degC/mW. Thus $T_j = 0{\cdot}25\times50+60°\text{C} = 72{\cdot}5°\text{C}$, and so I_{CBO}max for Tr_2 may safely be taken as 400µA for the following calculations.

The maximum voltage that will not trigger any BTZ18 is 0·25V, so that

$$R_4 < 0{\cdot}25\text{V}/400\mu\text{A} = 625\Omega.$$

Hence take $R_4 = 560\Omega\pm10\%$.

Taking h_{FE} as 30,

$$I_{b2}\text{min} = I_{c2}\text{max}/h_{FE}\text{min} = 3{\cdot}3\text{mA},$$

and taking V_{cc}min as 11V, and I_{CBO}max for Tr_1 at 60°C as 0·2mA,

$$R_2 \leqslant 2{\cdot}7\text{k}\Omega.$$

Thus $R_2 = 2{\cdot}2\text{k}\Omega\pm10\%$.

Taking V_{cc}max for Tr_1 as 13V and the lower limit of R_2,

$$I_{c1}\text{ max} = 13\text{V}/1{\cdot}98\text{k}\Omega = 6{\cdot}56\text{mA}.$$

Therefore

$$I_{b1}\text{min} = 6{\cdot}56\text{mA}/30 = 218\mu\text{A}.$$

Hence

$$R_3 < 10{\cdot}5/218 = 48\text{k}\Omega.$$

and

$$R_3 > 12{\cdot}5/25 = 500\Omega$$

where V_{be} is taken as 0·5V and I_{b1}max is 25mA.

A value of I_b within the above range may now be taken depending on the requirements discussed on p.142. For this example a value of 2·5mA will be taken. Hence $R_3 = 12/2{\cdot}5 = 4{\cdot}8\text{k}\Omega$.

Take $R_3 = 4{\cdot}7\text{k}\Omega\pm10\%$.

To limit the base current of Tr_1 to within the peak rating (50mA) while charging C,

$$R_5 > \frac{13}{50\times10^{-3}-\dfrac{13}{4230}} - 108 = 169\Omega.$$

Thus let $R_5 = 220\pm10\%$.

Finally, to obtain a 2ms pulse duration $t \simeq 0{\cdot}7CR_3$ which gives

$$C \simeq 0{\cdot}61\mu\text{F}.$$

Take $C = 0{\cdot}6\mu$F.

Practical Circuit (1)

For firing the types of SCR covered by this article, with a 2ms pulse, suitable component values are:

$R_1 = 1\text{k}\Omega\pm10\%$ $\qquad R_4 = 560\Omega\pm10\%$
$R_2 = 2{\cdot}2\text{k}\Omega\pm10\%$ $\qquad R_5 = 220\Omega\pm10\%$
$R_3 = 4{\cdot}7\text{k}\Omega\pm10\%$ $\qquad R_s = 120\Omega\pm10\%$
$C = 0{\cdot}6\mu$F

With the component values shown above the following results were obtained with an input of 5V from a 100Ω source.

Temperature (°*C*)	*Pulse duration* (*ms*)	*Sensitivity* (*V*/*µs*)
25	1·98	4·0
60	1·90	5·5

To show the effect of increasing R_3, its value was changed to 24kΩ and C to 0·1µF, that is $t = 0{\cdot}7CR = 0{\cdot}7\times0{\cdot}1\times24 = 1{\cdot}68$ms.
The results, with an input of 2V from a 100Ω source, were

Temperature (°*C*)	*Pulse duration* (*ms*)	*Sensitivity* (*V*/*µs*)
25	1·70	1·0
40	1·62	1·4
60	1·4	1·7

If a silicon transistor (for example, the OC200) is used for Tr_1, it is possible to increase R_3 to 47kΩ because of the reduction in I_{CBO}max. The sensitivity can be increased to 0·1V for 1µs at 25°C ambient temperature and the pulse duration maintained substantially constant up to 60°C.

Design Example (2)

With a supply voltage of 12V±10% it is required to produce a 2ms pulse to fire a type BTY64 SCR.

Assume the diode voltage drop for the current which flows when Tr_2 is bottomed, and the bottoming voltage of Tr_2, to be 1·5V. Hence the source voltage $V_s = 12-1{\cdot}5 = 10{\cdot}5$V.

From the design curves for 50% duty cycle, $R_s = 33\Omega\pm10\%$ and $V_s = 10{\cdot}5\text{V}\pm16\%$. The maximum allowable range of V_s is therefore from 8·8V to 12·2V. The practical range of V_s is from 9·3V to 11·7V, which is permissible. Therefore $I_c$max in Tr_2 will be $11{\cdot}7\text{V}/30\Omega = 390$mA, and with a maximum bottoming voltage of 0·5V the dissipation in Tr_2 will be 195mW when switched on. To use ACY20 transistors at ambient temperatures up to 45°C without additional heatsinks, the mark-to-space ratio should be 1:1, or less.

We also have the condition that V_D must be greater than 0·5V. A current of 10mA in an OA210 diode will give this voltage drop. Therefore

$$R_1 \leqslant 12\text{V}/10\text{mA} \leqslant 1{\cdot}2\text{k}\Omega.$$

Therefore let

$$R_1 = 1{\cdot}0\text{k}\Omega \pm 10\%.$$

At the maximum junction temperature, $I_{CBO}\text{max}$ is 500µA for an ACY20 transistor. The maximum voltage that will not trigger any BTY64 is 0·25V, so that, from Eq.(12).

$$\begin{aligned} R_4 &< V_{NF}/I_{CBO}\text{max} \\ &< 0{\cdot}25\text{V}/0{\cdot}5\text{mA} < 500\Omega. \end{aligned}$$

Let

$$R_4 = 470\Omega \pm 10\%.$$

If we take $h_{FE}\text{min}$ as 30,

$$I_{b2}\text{min} = I_{c2}\text{max}/h_{FE}\text{min} = 390/30 = 13\text{mA},$$

and if $V_{cc}\text{min}$ is 10·8V, and $I_{CBO}\text{max}$ for Tr_1 at 45°C is 0·2mA,

$$R_2 < \frac{V_{cc}\text{min} - (V_D + V_{be}\text{max})}{I_{b2}\text{min} + I_{CBO}\text{max}}. \qquad \text{(Eq.(14))}$$

Therefore

$$R_2 < (10{\cdot}8 - 1{\cdot}5)/(13{\cdot}2 \times 10^{-3}) < 700\Omega.$$

Let

$$R_2 = 610\Omega \pm 10\%.$$

$$I_{c1}\text{max} = V_{cc}\text{max}/R_2\text{min} = 13{\cdot}2/550 = 24\text{mA}.$$

Therefore

$$I_{b1}\text{max} = 24/30 = 800\mu\text{A}.$$

Therefore from Eqs.(15) and (16)

$$(V_{cc}\text{min} - V_{be})/I_{b1}\text{min} > R_3 > (V_{cc}\text{max} - V_{be})/I_{b1}\text{max}.$$

Hence

$$10{\cdot}3\text{V}/800\mu\text{A} > R_3 > 12{\cdot}7\text{V}/25\text{mA}$$

where $I_{b1}\text{max} = 25\text{mA}$ for an ACY20 transistor.
Therefore

$$12{\cdot}9\text{k}\Omega > R_3 > 510\Omega.$$

A value of I_b within the above range may now be chosen, depending on the requirements discussed on p.142. In this example a value of 5mA will be taken. Therefore

$$R_3 = 12\text{V}/5\text{mA} = 2{\cdot}4\text{k}\Omega.$$

Let

$$R_3 = 2{\cdot}2\text{k}\Omega \pm 10\%.$$

From Eq.(13)

$$R_5 > \frac{V_{cc}\text{max}}{I_{b1}\text{max} - \dfrac{V_{cc}\text{max}}{R_3\text{min}}} - R_s\text{min}.$$

Therefore

$$R_5 > \frac{13{\cdot}2}{50 \times 10^{-3} - \dfrac{13{\cdot}2}{1980}} - 30 > 275\Omega.$$

Let

$$R_5 = 330\Omega \pm 10\%.$$

From Eq.(16)

$$t \simeq 0{\cdot}7CR_3.$$

Therefore for a 2ms pulse duration

$$C = (2 \times 10^{-3})/(0{\cdot}7 \times 2{\cdot}2 \times 10^3) = 1{\cdot}3\mu\text{F}.$$

Then

$$C = 1{\cdot}5\mu\text{F}.$$

Practical Circuit (2)

Suitable values for the circuit of Fig. 2 are:

$R_1 = 1\text{k}\Omega$ $R_4 = 470\Omega$
$R_2 = 610\Omega$ $R_5 = 330\Omega$
$R_3 = 2{\cdot}2\text{k}\Omega$ $R_s = 33\Omega$
$C = 1{\cdot}5\mu\text{F}$
$D = \text{OA210}$
$Tr_1, Tr_2 = \text{ACY20}$
All resistors are ±10% tolerance.

This circuit requires an input pulse of 1V amplitude, 5µs duration. If some form of heatsink is used, ACY20 transistors can be used at higher ambient temperatures than 45°C.

Triggered Blocking Oscillators

Design Example (1) (Fig. 3)

It is required to produce a pulse of 200µs duration, to fire a BTZ19 type SCR. A supply of 9V±1V is available. The value of n_1/n_2 must be greater than unity, but low enough to produce a voltage across n_2 that is about 10 times V_{be}. The value chosen will affect trigger sensitivity, and will be determined later by substituting values in Eq.(19).
Let

$$n_1/n_2 = 2.$$

Assuming $V_{CE(\text{knee})} = 1\text{V}$, V_{n1} can be calculated from Eq.(18).

$$V_{n1} = \frac{9-1}{1-0{\cdot}5} = 16\text{V}.$$

From the SCR design curves (25% duty cycle) it can be seen that for a source resistance of 150Ω±10%, the source voltage is 14V±44% to fire every BTZ19 under the most adverse conditions. This therefore includes the 16V given above.

A value of L_{n1} must now be chosen. If this is made 50mH, it will give a change of current of about 60mA during the required pulse period and this can be accommodated on the chosen transformer core. A suitable core for the transformer is Ferroxcube FX1238. The number of turns required on this core is given by

$$n = 32\sqrt{L}$$

where L is in mH.
This gives

$$n_1 = 220 \text{ turns}, \quad n_2 = 110 \text{ turns}.$$

It is advisable to minimise leakage inductance and winding resistance so that the practical circuit will approach as closely as possible the design calculations. This can be achieved by bifilar winding and by use of the largest gauge of wire that the bobbin will hold.
From Eq.(20)

$$r_{ie} = 22\Omega$$

and from Eq.(25),

$$I_e = 360\text{mA}.$$

For an ACY20 transistor, take h_{FE} as 20 for design purposes, giving

$$(1-\alpha)/\alpha = 0{\cdot}05, \text{ and } \alpha = 0{\cdot}95.$$

Thus from Eq.(22), using a typical $r_{bb'} = 60\Omega$,

$$R_b < 380\Omega.$$

Hence let $R_b = 330\Omega$.

To determine the value of base current at which the circuit will fire, the expression for loop gain (Eq.(19)) can be used, with $I_c = 2\text{mA}$.
From published data for the ACY20, $h_{FE}\text{min} = 28$ and so

$$\alpha = 0{\cdot}965 \text{ and } I_b = 0{\cdot}072\text{mA}$$
$$(1-\alpha) = 0{\cdot}035.$$

From Eq.(19)

$$\text{Loop gain} = \frac{0{\cdot}965 \times 150 \times 2}{4(0{\cdot}035)(348+60+330)+150} = \frac{290}{253}$$

This is slightly greater than unity, and thus the circuit will trigger when $I_b \simeq 0{\cdot}07\text{mA}$. Eq.(24) can be used to calculate the current required from the driving pulse.

$$r_i = 0{\cdot}25 \times 250 \times 28 = 1750\Omega.$$

Let $V_e = 0{\cdot}5\text{V}$.
Then $I_{in} = 2{\cdot}2\text{mA}$.

Thus if a 5V pulse is available, $R_1 \simeq 2\text{k}\Omega$. Let $R_1 = 1{\cdot}8\text{k}\Omega \pm 10\%$. The recovery time must now be calculated.

The maximum reverse gate voltage rating of the BTZ19 is −10V, and from Eqs.(26) and (27),

$$R_3 = 10\text{V}/250\text{mA} = 40\Omega.$$

Let

$$R_3 = 33\Omega \pm 10\%,$$

then the recovery time $= 4 \times 50 \times 10^{-3}/33 = 6{\cdot}0\text{ms}$.

The temperature stabilising diode D_1 should run at a current of about 15mA. Therefore $R_2 = 560\Omega$.

Practical Circuit (1)

For firing the types of SCR covered by this article with a 200µs pulse, suitable component values are

$V_{cc} = 9\text{V} \pm 1\text{V}$ $R_3 = 33\Omega \pm 10\%$
$R_1 = 1{\cdot}8\text{k}\Omega \pm 10\%$ $R_b = 330\Omega \pm 10\%$
$R_2 = 560\Omega \pm 10\%$ $R_s = 150\Omega \pm 10\%$
n_1/n_2 = 220/110 turns on core FX1238 (2 off)
Transistor = ACY20
D_1 = OA200
D_2 = OA200

Variants of Basic Circuit

(i) It is possible to take the output of this circuit from an isolated third winding. The load would then be transferred to a third winding n_3 equal in turns to n_1, the rest of the circuit remaining unchanged. In this case the winding resistance can be high, provided that its value is subtracted from the value of R_s used.

(ii) The recovery time of the circuit can be reduced by adding a diode in series with R_s. The value of R_3 can be increased, thus allowing the voltage on the collector to rise higher and to be limited only by the maximum transistor voltage rating.

When determining R_3, the maximum reverse gate voltage rating of the SCR should not be used in Eq.(27.) Instead, use either the maximum collector-base voltage rating of the transistor, less V_{cc}; or the maximum emitter-base voltage rating times n_1/n_2. The lower of these values should be used.

For the worked example on page 152 with an ACY20 transistor and $n_1/n_2 = 2$,

$$R_3 \leqslant (32-10\text{V})/250\text{mA} \quad \text{or} \quad R_3 \leqslant 12\text{V} \times 2/250\text{mA}$$

With the lower value, $R_3 = 68\Omega \pm 10\%$ is suitable.

$$\text{Recovery time} = \frac{4 \times 50 \times 10^{-3}}{68} = 2{\cdot}9\text{ms}.$$

This time can be reduced still further by supplying more trigger current.

Design Example (2) (Fig. 4)

It is required to extend and amplify a 20µs pulse sufficiently to fire a type BTY64 SCR. A supply voltage of 12V±10% is available.

From Eq.(29)

$$V_{n1}\text{max} = 13{\cdot}2 - 0{\cdot}5 = 12{\cdot}7\text{V}.$$

From Eq.(30)

$$V_{n1}\text{min} = 10{\cdot}8 - 0{\cdot}5 - 0{\cdot}5 = 9{\cdot}8\text{V}.$$

Taking the mean of these two values we have

$$V_s = 11{\cdot}25\text{V}.$$

From the 50% duty cycle design curves, $R_s = 39\Omega \pm 10\%$, and the tolerance on V_s is ±16%. This gives a range of V_s of from 9·45V to 13·05V which covers the range of V_{n1} and is therefore permissible.

At a junction temperature, T_j, of 80°C, $I_{CBO} = 0{\cdot}4\text{mA}$ for an ACY20 transistor.

Then from Eq.(31)

$$\begin{aligned} R_2 &\leqslant (0{\cdot}5 - 0{\cdot}2)/(0{\cdot}4 \times 10^{-3}) \\ &\leqslant 750\Omega. \end{aligned}$$

Thus let $R_2 = 680\Omega$.

The diode D_2 (OA200) should be operated at about 10mA to give the required forward voltage drop.
Therefore

$$R_3 \leqslant (V_{cc}\text{min} - V_{D2})/10\text{mA} \leqslant (10{\cdot}3)/10 \times 10^{-3} \leqslant 1030\Omega.$$

Thus take $R_3 = 1\text{k}\Omega$.

Limiting $I_{n1(\text{final})}$ to 50mA, choosing H = 3 oersted for core saturation, and using the Ferroxcube FX1105 core for which $\ell = 5{\cdot}6\text{cm}$, we have, from Eq.(33)

$$n = (3 \times 10 \times 5{\cdot}6)/(4\pi \times 50 \times 10^{-3}).$$

Therefore

$$n = 268 \text{ turns}.$$

Also

$$L_{n1} = (n/K)^2$$

where K is the ‘turns for 1mH’ parameter of the core used.
Therefore

$$\begin{aligned} L_{n1} &= (268/20)^2 \\ &= 180\text{mH}. \end{aligned}$$

Then from Eq.(32)

$$t_p = (180 \times 10^{-3} \times 50 \times 10^{-3})/12 = 750\mu\text{s}.$$

From Eq.(39) we have

$$\frac{12{\cdot}2}{35}N^2 + 50 \times 10^{-3}N^2 - \frac{11{\cdot}25 \times 30}{680}N + \frac{12{\cdot}2}{610} = 0$$

whence

$$N = 1{\cdot}2 \text{ or } 0{\cdot}05.$$

N = 1·2 is the only practical solution, and so let N = 1.

The voltage drop from the base of the transistor to earth is (0·5+1·0)V, therefore let

$$V_1 = 2{\cdot}5\text{V} \text{ and } V_2 = 2{\cdot}0\text{V}.$$

From Eq.(40), with $R_1 = 1000\Omega$

$$C = 20.10^{-6}/\left(1000.\log_e\frac{2{\cdot}5}{2{\cdot}0}\right) = 0{\cdot}1\mu\text{F}.$$

From Eq.(42)

$$h_{FE(\text{lim})} = (680+39)/39 = 18.$$

The collector current for the ACY20 which gives this value of h_{FE} is less than 1mA.

Therefore the base drive required $< 1\text{mA}/18 \simeq 50\mu\text{A}$.

Practical Circuit (2)

$V_{cc} = 12\text{V} \pm 10\%$ $R_2 = 680\Omega$
$C = 0{\cdot}1\mu\text{F}$ $R_3 = 1\text{k}\Omega$
$R_1 = 1\text{k}\Omega$ $R_s = 39\Omega$
All resistors ±10%
Transistor = ACY20 Transformer:
D_1, D_2, D_4, D_5 = OA200 Core = FX1105 (2 off)
D_3 = OAZ230, SZ12C $n_1/n_2 = 1:1$
Collector winding turns = 270 turns 36 s.w.g. Cu. En.
Collector winding inductance = 180mH.

The circuit will work at frequencies up to 400c/s, and requires a pulse input for reliable operation of 2·5V, 50µA.

Variants of Basic Circuit

(i) The circuit shown in Fig. 4 may be simplified in a number of ways, although any simplification will have a detrimental effect upon the circuit performance.

(a) The input may be fed directly into the base, although for long input pulses a.c. coupling is imperative, or the transistor will be overloaded.

(b) If a.c. coupling is used, diode D_1 provides a discharge path for C. Otherwise, C would not have time to discharge completely through R_1, R_2 and n_2 before the next input pulse. This would lower the maximum frequency of operation of the circuit.

(c) If a zener diode D_3 is used in conjunction with an ordinary diode, D_4, the overswing across the collector winding can be limited to a safe value given by the transistor rating. The recovery time of the overswing is also shortened, and hence the frequency of operation is increased.

(d) Diode D_5 shortens the recovery time of the circuit and prevents negative voltages being applied to the SCR gate.

(e) The value of R_1 is chosen arbitrarily, a high value giving a good recovery time but lower sensitivity, and *vice versa*.

(ii) Fig. 9 shows an arrangement which could be used to vary the output pulse duration. Increasing RV_1 reduces the pulse duration, while R_4 is a compromise between temperature stability and regeneration requirements.

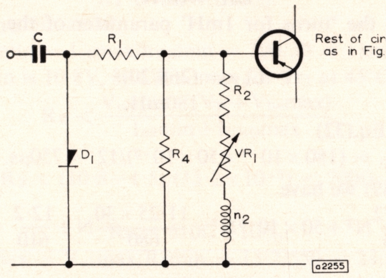


Fig. 9—Triggered blocking oscillator giving variable pulse duration

The regeneration equation for this circuit is:

$$(VR_1+R_2) \leqslant \frac{R_4(h_{FE}R_s-Nr_{bb'})}{N(r_{bb'}+R_4)}-\frac{R_s}{N^2}.$$

Suitable additional component values for this circuit are:

$$RV_1 = 100\Omega,\ R_4 = 680\Omega\pm10\%.$$

All other values are as for the circuit of Fig. 4.

Free-running Blocking Oscillator (Fig. 5)

Design Example

It is required to fire a BTZ18 type SCR with 50μs firing pulses, with a supply voltage of 12V±2V. From the firing-circuit design curves it can be seen that for a BTZ18 fired through a resistance R_s of 82Ω±20%, a voltage tolerance of 9·5V±48% is allowable.

Thus the minimum firing voltage $V_s\text{min}$ is 52% of 9·5V, that is, 5V.

With $V_b = 7{\cdot}5V$, the pulse output could be 6V with low supply voltage. The time-constant CR_s must be such that this voltage does not decay to less than 5V in 50μs.

From Eq.(44)

$$C = \frac{50\times10^{-6}}{(82\times0{\cdot}8)\ \log_e\frac{6}{5}} = 4{\cdot}2\mu F.$$

Therefore take $C = 4\mu F$.

If an ACY20 transistor is used and the circuit is designed for a maximum leakage current of 1mA, Eq(45) gives

$$(1\times10^{-3}R_2R_3)/(R_2+R_3) = 0{\cdot}2V,$$

and Eq.(46) gives

$$V_b = 12R_3/(R_2+R_3) = 7{\cdot}5V.$$

From these two equations

$$R_2 = 320\Omega \text{ and } R_3 = 530\Omega.$$

The nearest preferred values are

$$R_2 = 330\Omega \text{ and } R_3 = 560\Omega.$$

Thus

$$R_b = (330\times560)/(330+560) = 210\Omega.$$

The maximum base current for the ACY20 is 50mA. From Eq.(47), with the supply voltage high, and with this base current,

$$n_2/n_1 = (50\times10^{-3}\times210)/8{\cdot}8 = 1{\cdot}2.$$

Let $n_2/n_1 = 1:1$, giving a maximum base current of 42mA. The capacitor will discharge from V_b down to V_c, given by Eq.(48).

$$V_c = 7{\cdot}5/(1+1) = 3{\cdot}75V.$$

Eq.(50) gives the pulse duration

$$t_p = \frac{4\times10^{-6}\times(R_g+82)\times210}{R_g+82+210}\log_e\frac{7{\cdot}5}{3{\cdot}75}$$

$$\simeq 160 \text{ to } 270\mu s, \text{ depending on the value of } R_g.$$

From Eq.(51), the initial primary current I_{n1} is given by

$$I_{n1} = 7{\cdot}5(1{\cdot}0)^2/210 = 36mA.$$

From Eq.(52)

$$L_{n1} \geqslant (7{\cdot}5\times270\times10^{-6})/(0{\cdot}50\times36\times10^{-3}) = 112mH.$$

For a minimum emitter current of 1mA, from Eq.(53),

$$R_1 = 4{\cdot}5k\Omega \text{ (Maximum)}.$$

The minimum h_{FE} required for regeneration at $I_e = 1mA$ can be found by taking a typical value of 60Ω for $r_{bb'}$, and using Eq.(54),

$$h_{FE}\text{min} = \frac{(1{\cdot}0)^2(270)+82}{1{\cdot}0(82-25)} = 6.$$

The h_{FE} for the ACY20 at 1mA collector current is always well above this value. If $R_1 = 3{\cdot}9k\Omega$, then t_{charge} is given by Eq.(55),

$$t_{\text{charge}} = 4\times10^{-6}\times3{\cdot}9\times10^3\log_e\frac{12-3{\cdot}75}{12-7{\cdot}5} = 9ms.$$

Practical Circuit

For firing the types of SCR covered by this article, suitable component values are as follows

V_{cc} = 12V±2V

R_1 = 3·9kΩ for pulse duration 200μs, charging time 9·0ms

R_2 = 330Ω±10%

R_3 = 560Ω±10%

R_s = 82Ω±20%

C = 4μF

Pulse transformer turns ratio = 1:1 (330 turns each winding)

Core = FX1238 (two off)

Winding inductance = 120mH

Diode = OA200

Transistor = ACY20

Variants of Basic Circuit

(i) If the supply to the blocking oscillator is from a zener diode across the SCR, as shown in Fig. 10, the circuit can be used for firing a half-wave phase-controlled rectifier, using the time-constant $C.RV_1$ to delay the firing pulse applied to the SCR. Thus, by adjusting RV_1, the SCR can be made to conduct for varying portions of each half cycle.

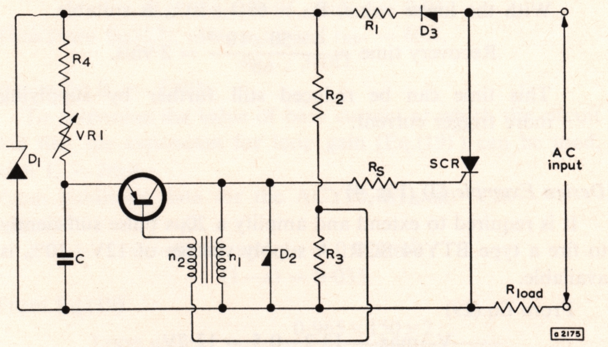


Fig. 10—Free-running blocking oscillator with phase control

The circuit operation when the transistor is non-conducting is similar to that already described. The blocking oscillator will regenerate when the voltage across C just exceeds the bias voltage. When the blocking oscillator triggers, a pulse is fed to the SCR gate and the anode-cathode voltage of the SCR falls to about 1V. This means that the hold-off bias to the base of the transistor has been removed, and the oscillator will continue to oscillate because of the voltage on the capacitor C. Thus C is rapidly discharged and the circuit is dormant until the start of the next positive half cycle.

Diode D_3 is included to prevent spurious firing of the blocking oscillator which may be caused by the small negative voltage developed across D_1. This voltage takes the base of the transistor rapidly negative, while the emitter potential rises more slowly. Without D_3, this would result in spurious pulses.

The resistor R_4 in series with RV_1 prevents excessive loading of the zener voltage waveform by the timing capacitor.

Suitable component values for the circuit of Fig. 10 for 50c/s phase control of the BTZ19 from a 110V (r.m.s.) a.c. input are:

R_1 = 1·8kΩ, 3W

R_2 = 340Ω

R_3 = 1·0kΩ

R_4 = 82Ω

R_s = 68Ω

RV_1 = 10kΩ

C = 2μF

Tr = ACY20

D_1 = OAZ207

D_2, D_3 = OA200

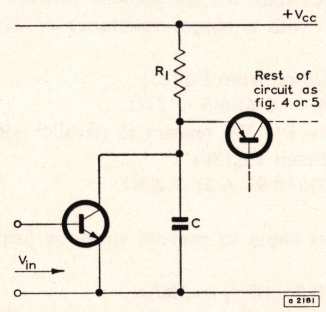
Pulse transformer turns ratio = 180 turns each winding

Core = FX1238 (two off)

Winding inductance = 36mH

For different values of a.c. input, the appropriate value of R_1 must be chosen.

(ii) The rate of charging of C in Figs. 5 and 10 can also be controlled by a transistor directly across it as shown in Fig. 11.



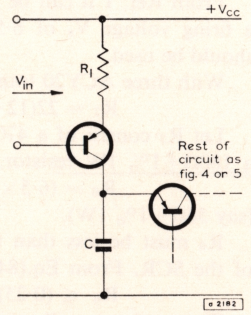


Fig. 11—Transistor control of free-running blocking oscillator

Fig. 12—Alternative transistor control of free-running blocking oscillator

This arrangement can be used when the input is common to the earth line.

Alternatively, the rate of charging of C can be controlled by a transistor in series with R_1, as shown in Fig. 12. This arrangement can be used when the transistor input is common to the positive supply of the firing circuit.

(iii) The basic circuit can conveniently be adapted to feed a number of isolated outputs simply by adding further windings to the transformer.

Schmitt Circuits

Design Example (1) (Fig. 6)

Given a supply of 12V, it is required to fire a type BTZ18 SCR when the input voltage level reaches 4·0V.

For two ACY20 transistors with a maximum bottoming voltage of 0·5V, Eq.(56) gives

$$V_s = 11{\cdot}5V.$$

From the firing curves in Ref. 1 for 100% duty cycle, the required $R_s = 120\Omega$. Thus from Eq.(57)

$$R_4+R_5 = 120\Omega\pm10\%.$$

If we take the lowest SCR gate impedance and if Tr_2 is intended to bottom when resistors are −10%,

$$Ic_2 = 11{\cdot}5/108 = 106mA.$$

Then from Eqs.(58) and (59)

$$I_{b2} = 106/50 = 2{\cdot}1mA.$$

From Eq.(60)

$$I_{R1R2R3} = 21mA.$$

Therefore

$$R_1+R_2+R_3 = 12V/21mA = 570\Omega.$$

Since it is required that the SCR should fire when the input voltage level is 4V, let V_e equal 7V when Tr_2 is just bottomed. Then, from Eq.(62)

$$R_3 = (7+0{\cdot}4V)/21mA = 350\Omega.$$

Thus, let $R_3 = 330\Omega\pm10\%$.

From Eq.(63)

$$R_4 = 7V/106mA = 66\Omega.$$

Then let $R_4 = 68\Omega$.

From Eq.(57)

$$R_5 = 120-68 = 52\Omega.$$

Thus, let $R_5 = 47\Omega$.

From Eq.(65)

$$R_1 = \frac{12\times330\times68-68\times570\times4{\cdot}0}{440\times330}\Omega$$

$$= 86\Omega.$$

Therefore let $R_1 = 82\Omega$.

Then from Eq.(66)

$$R_2 = 570-(82+330) = 158\Omega.$$

Therefore let $R_2 = 150\Omega$.

From Eq.(67)

$$R_{ss} \leqslant (50\times68)/10\Omega,$$

that is

$$R_{ss} \leqslant 340\Omega.$$

With minimum loop gain and the worst arrangement of ±10% resistors, then Eq.(69) gives

$$\beta = \frac{61}{61+165+363} = \frac{1}{9{\cdot}7}.$$

In Eq.(70), take the maximum value of $r_{bb'}$ as 3 times the typical value given in published data ($r_{bb'} = 180\Omega$), and the −10% tolerance on R_3;

then $r_{e1} = 25/I_{e1} = 25/80mA = 0{\cdot}31\Omega$ where

$$I_{e1} = V_{cc}/(R_1+R_4)$$

and $r_{e2} = 25/I_{e1} = 25/10 = 2{\cdot}5\Omega$ where I_{e2} is an arbitrary value. Therefore

$$r_{e1}+r_{e2} = 2{\cdot}8\Omega.$$

Since $\beta = 1/9{\cdot}7$, A must be $\geqslant 9{\cdot}7$ and an adequate value for A for calculation purposes would be 10.

From Eq.(70)

$$R_{ss}\text{max} = \frac{50\times300-10(830)}{10} = 820\Omega.$$

Thus the value for R_{ss} should be that obtained from Eq.(67), that is $R_{ss} \leqslant 340\Omega$ (use $R_{ss} = 330\Omega$).

The $I_{CBO}\text{max}$ of an ACY20 is 0·5mA at 85°C. Thus from Eq.(71),

$$R_6 = 0{\cdot}25/(0{\cdot}5\times10^{-3}) = 500\Omega$$

and so we may take $R_6 = 470\Omega$.

Practical Circuit (1)

Suitable practical components for the circuit of Fig. 6 are thus:

V_{cc} = 12V (stabilised)

R_1 = 82Ω

R_2 = 150Ω

R_3 = 330Ω

R_4 = 68Ω

R_5 = 47Ω

R_6 = 470Ω

R_{ss} = 330Ω (including supply)

Tr_1, Tr_2 = ACY20

The circuit will always operate with ±10% tolerance resistors, but with this set of values the value of V_{on} could vary by a maximum of ±15%. Also V_{on} will vary with V_{cc}, to which it is proportional. Thus to maintain the value of V_{on} the component R_4 in Eq.(63) must be appropriately low-tolerance.

Design Example (2) (*Schmitt circuit with Specific Backlash*) (Fig. 7)

It has been found that a value of V_{cc} greater than 12V simplifies tolerancing problems in this circuit. Let $V_{cc} = 15V$.

With a 1V drop across Tr_3 when supplying a short-circuit gate, 14V remain for applying to R_s and the SCR gate. From the SCR design curves for 100% duty cycle it can be seen that $R_s = 220\Omega \pm 10\%$ is a suitable value. R_9 is equivalent to R_s in this circuit.

Thus

$$R_9 = 220\Omega \pm 10\%.$$

From Eq.(72)

$$V_{b4}max = 15-(2+0\cdot5) = 12\cdot5V.$$

From Eq.(73)

$$I_{c3}max = (15-0\cdot5)/200 = 73mA.$$

Thus

$$I_{b3} = 73mA/50 = 1\cdot5mA.$$

From Eq.(75)

$$R_5max = (1-0\cdot5)/1\cdot5 = 330\Omega.$$

Thus let

$$R_5 = 300\Omega \pm 5\%.$$

From Eq.(76)

$$I_{c4}max = 12\cdot5/200 = 62mA.$$

From Eq.(77)

$$R_6+R_7 = 750/620 = 1\cdot21k\Omega.$$

From Eq.(78)

$$R_7 = 12\cdot5R_6/2\cdot5$$
$$R_7 = 5R_6$$
$$R_6 = 1\cdot21/6 = 201\Omega$$

and

$$R_7 = 1210-201 = 1009\Omega.$$

Since Eqs.(77) and (78) use $V_{b4}max$, the practical values for R_6 and R_7 should be such as to give a value of V_{b4} slightly less than the maximum.

Thus

$$R_6 = 220\Omega \pm 5\% \text{ and } R_7 = 1k\Omega \pm 5\%.$$

From Eq.(79)

$$R_8max = \frac{15-(12\cdot5+1)}{62\times10^{-3}} = 24\Omega.$$

Thus let

$$R_8 = 22\Omega.$$

R_8 can be a 10% tolerance resistor.

With an emitter voltage variation of from 5·5 to 7V, the minimum value for V_{c2} is 8V. We will set the maximum value for V_{c2} at 11V. Then from Eqs. (80) and (81)

$$I_{c2}max = (15-8)/315 = 22mA$$

and

$$I_{c2}min = (15-11)/285 = 14mA.$$

and from Eqs.(82) and (83)

$$R_4max = 5\cdot5/0\cdot014 = 393\Omega$$
$$R_4min = 7/0\cdot022 = 318\Omega.$$

A suitable value between these is 360Ω with a tolerance of ±5%.

Let the current through $R_1+R_2+R_3$ be 5mA. Since V_e varies from 5·5 to 7V, it is reasonable to allow a variation from 6V to 7V at the base of Tr_2.

This means a nominal V_{b2} of 6·5V.

$$R_3 = 6\cdot5/0\cdot005 = 1\cdot3k\Omega.$$

However, the preferred value of 1·2kΩ gives a current through $R_1+R_2+R_3$ of 5·4mA. Thus

$$R_1+R_2+R_3 = 15/5\cdot4mA = 2\cdot78k\Omega.$$

The SCR will fire when the input is raised to the Schmitt emitter voltage. Let the input level at which the SCR gate voltage is removed, V_{off} be 4V.

Then from Eq.(65)

$$R_1 = \frac{15\times1\cdot2\times360-360(2\cdot78)4}{4\times1\cdot2} = 520\Omega.$$

Let $R_1 = 510\Omega \pm 5\%$

and then $R_2 = 2\cdot78k\Omega-1710\Omega = 1\cdot07k\Omega.$

Let $R_2 = 1k\Omega \pm 5\%$.

The SCR will fire when the input is raised to the Schmitt emitter voltage existing when Tr_2 is conducting.

This is given by

$$V_{on} = (V_{cc}R_3)/(R_1+R_2+R_3)$$
$$= (15\times1\cdot2)/(510+1\cdot0+1\cdot2) = 6\cdot65V.$$

From Eq.(64)

$$V_{on} = \frac{15\times1\cdot2\times0\cdot36}{0\cdot36\times2\cdot71+0\cdot51\times1\cdot2}$$
$$= 3\cdot85V.$$

The value of R_{10} is the same as that of R_6 in the basic Schmitt trigger circuit, that is, $R_{10} = 470\Omega$.

Practical Circuit (2)

Suitable component values for this circuit are:

$V_{cc} = 15V$ (stabilised)
$R_1 = 510\Omega \pm 5\%$ $R_2 = 1k\Omega \pm 5\%$
$R_3 = 1\cdot2k\Omega \pm 5\%$ $R_4 = 360\Omega \pm 5\%$
$R_5 = 300\Omega \pm 5\%$ $R_6 = 220\Omega \pm 5\%$
$R_7 = 1k\Omega \pm 5\%$ $R_8 = 22\Omega \pm 10\%$
$R_9 = 220\Omega \pm 10\%$ $R_{10} = 470\Omega \pm 10\%$
All transistors are ACY20.

Design Example (3) (*Schmitt circuit with amplifier Fig. 8*)

Given a 12V supply it is required to design the circuit to fire all SCRs in the BTY64 range.

From Ref. 1 it can be seen that, for the greatest tolerance, a firing voltage V_s of 6·5V with a source resistance of 22Ω should be used.

With three ACY20 transistors, from Eq.(85)

$$R_7 = 22(12-0\cdot7-0\cdot4)/6\cdot5 = 37\Omega.$$

Let R_7 consist of a 470Ω±1% 3W resistor in parallel with a 180Ω±1% 1W resistor. From Eq.(86)

$$R_6 = (6\cdot5\times37)/(10\cdot9-6\cdot5) = 55\Omega$$

(say 56Ω±1% 1W).

R_6 must be less than this value to prevent spurious firing of the SCR. From Eq.(84)

$$R_6 \leqslant (0\cdot25)/(0\cdot5\times10^{-3}) = 500\Omega.$$

The maximum collector current, I_{c3}, required to bottom Tr_3 (from Eq.(87)) is

$$I_{c3}max = (12-0\cdot5-0\cdot1)/37 = 308mA.$$

Therefore

$$I_{b3} = 308mA/30 = 10\cdot3mA.$$

Let $I_{b3} = 11mA$.

From Eq.(88)

$$R_8 = (0\cdot5-0\cdot2)/0\cdot5mA = 600\Omega.$$

Hence let $R_8 = 560\Omega \pm 10\%$ ¼ watt. The forward voltage drop across an OA210 diode is at least 0·5V for currents greater than 10mA. Thus

$$R_9 = 12V/10mA = 1200\Omega.$$

An OAZ269 giving a zener voltage spread from 4·4V to 6V is suitable for D_2.

To be certain that the collector voltage of Tr_2 falls below 4·4V when conducting, it is safe to consider an emitter voltage, V_{e2}, of 3V.

From Eq.(89)

$$R_5 = \frac{6\times500-11\times10^{-3}\times500\times60}{11\times10^{-3}\times(500+60)}$$
$$= 435\Omega.$$

Therefore to ensure sufficient base drive, let

$$R_5 = 390\Omega \pm 1\%, \tfrac{1}{4}W.$$

The maximum collector current of Tr_2 is given by

$$I_{c2} = (12-3)/390 = 23mA$$

and so

$$I_{b2} = 23/50 = 0\cdot46mA.$$

From this point it is convenient to use the information and equations for the basic Schmitt circuit.

From Eq.(60)

$$I_{R1R2R3} = 4\cdot6mA.$$

Let $I_{R1R2R3} = 5mA$, then

$$R_1+R_2+R_3 = 12/5mA = 2400\Omega \text{ (Eq.(61))}$$
$$R_3 = 3\cdot3/5mA = 660\Omega \text{ (Eq.(62))}.$$

Thus let $R_3 = 680\Omega \pm 1\%$.

$$R_4 = 3/23mA = 130\Omega \text{ (Eq.(63))}.$$

This can be made up from a 150Ω±1% resistor in parallel with a 1kΩ±1% resistor.

The SCR will fire when the input voltage is slightly above I_e. This will be 3·2V, approximately.

If the signal is to be removed from the gate when the input is at 2V then R_1 can be calculated from Eq.(64).

$$R_1 = (12\times680\times130-130\times2{,}400\times2)/(2\times680) = 320\Omega.$$

Let $R_1 = 330\Omega \pm 1\%$.

Hence

$$R_2 = 2400\Omega-330\Omega-680\Omega = 1390\Omega.$$

If high stability resistors are used, the triggering voltages are consistent, and maximum tolerance in V_{cc} is available.

From Eq.(67) the maximum value of signal source resistance R_{ss} can be calculated.

$$R_{ss} \leqslant 50\times130/10 = 650\Omega.$$
$$(h_{FE} = 30)$$

The open-loop gain A of the circuit can now be calculated from Eq.(68).

$$A = (50+680)/(360+50[25]+650+680) = 11\cdot5.$$

From Eq.(69)

$$\beta = 320/2400 = 1/7\cdot5.$$

Since $A\beta \geqslant 1$, the circuit will always be regenerative.

The power dissipation (P_3) in Tr_3, when it is bottomed, is given by the product of bottoming voltage and collector current, that is

$$P_3 = 0\cdot5\times308 = 154mW.$$

From the published data, this dissipation is permissible up to an ambient temperature of 47°C. For operation at ambient temperatures up to 55°C, the thermal resistance junction ambient must be decreased to 0·175degC/mW or less by means of a small heatsink.

Practical Circuit

Suitable components for the circuit of Fig. 6 are:

V_{cc} = 12V (stabilised)
$R_1 = 330\Omega \pm 1\%$ $R_2 = 1390\Omega$
$R_3 = 680\Omega \pm 1\%$ $R_4 = 130\Omega$
$R_5 = 390\Omega \pm 1\%$ $R_6 = 56\Omega \pm 1\%$ 1W
$R_7 = 37\Omega$ (47Ω±1% 3W in parallel with 180Ω±1% 1W)
$R_8 = 560\Omega \pm 10\%$ $R_9 = 1\cdot2k\Omega \pm 10\%$
$R_{ss} \leqslant 650\Omega$ (including supply)
Tr_1, Tr_2, Tr_3 = ACY20
D_1 = OA210
D_2 = OAZ269

Switch-off Circuits for SCRs Operating on d.c.

R. A. Payne and E. S. Reeves
Mullard Semiconductor Measurement and Application Laboratory

Two circuits suitable for firing SCRs on d.c. supplies are described. Firing requirements for both resistive and inductive loads are discussed, and design procedure for practical circuits is explained. The first circuit may be considered as a power bistable circuit and the second as a chopper with the ability to switch off completely.

The following possible applications are suggested:

Circuit 1

Control for road traffic and pedestrian crossing lights; aircraft navigation lights; vibrator motors; processes and diaphragm pumps.

Circuit 2

Control for alternator fields; d.c. motors; crane electromagnets; magnetic couplings; regulated power supplies; constant current battery chargers; radar and cyclotron magnets; and electric arc furnaces.

INTRODUCTION

Operation of SCRs on d.c. supplies poses new problems in firing circuit design. On an a.c. supply, an SCR will extinguish automatically when the supply voltage falls to zero, thus reducing the current to below the holding value. It is obvious that this condition does not hold when the SCR is operated from a d.c. supply, and hence some provision must be made for switching off the SCR.

Switch-off could be accomplished by placing a diverting transistor or mechanical relay in parallel with the device, but this method would be unsatisfactory for SCRs with high current-handling capacities. It is also possible to place a capacitor in series with the SCR across the supply, so that the SCR becomes self-extinguishing. However, in this arrangement the value of capacitance used limits the duration of current flow, and hence the power which can be delivered.

The system which is most frequently used is that which employs a charged capacitor to commutate the conducting SCR, by means of an additional SCR.

SWITCH-OFF CIRCUITS USING TWO SCRs

The majority of switch-off circuits utilise two SCRs, the switching on of one applying a charged capacitor to the other, of such a polarity as to make the anode negative with respect to the cathode.

At the instant of switching, the reverse-biased SCR will pass a reverse current until the charge of the end regions of the device has been extracted. The magnitude of this current is difficult to assess, since its value is dependent upon the switching impedances of the SCRs used, the self-inductance and resistance of the circuit, and the voltage to which the commutating capacitor is charged.

Because of this reverse current flow, some charge will be lost from the commutating capacitor during this period. This means that the voltage across the reverse-biased SCR will not be as great as predicted. In general, however, the loss of the charge is not great enough to affect the calculation of the value of commutating capacitance. The only case where it may have significance is when the supply voltage is low (say <20V) and the current is high.

SCR Reverse Current Rating

Although the reverse current pulse lasts for only a few microseconds its value is important, since reverse current in excess of the maximum rating can lead to a marked deterioration of the SCR characteristics.

As the reverse current magnitude is to some extent dependent upon the value of forward current which had been flowing before commutation, this limitation is especially important for the BTY64 series of SCRs where the ratio maximum permissible reverse current/maximum average forward current is only 0·43 : 1 whereas, with the BTY27 series this ratio is 3·2 : 1.

SCR Reverse Current Measurement

It is highly advisable in any high-power circuit that the transient current waveform should be monitored, using a wideband oscilloscope and a low-value non-inductive resistance. If the reverse peak current is approaching the maximum rating of the SCR, some method of limiting it (for example, by the inclusion of a low value of inductance in series with the commutating capacitor) must be used.

Although the value of the monitoring resistor must be low for high-current circuits it is equally essential that the ratio of self-inductance/resistance is also low. As the rate of change of current may exceed 10^7A/s during the switch-off, it is obvious that accurate measurement of this current change is difficult.

SCR BISTABLE CIRCUIT

The simplest practical circuit using two SCRs is the bistable circuit illustrated in Fig. 1.

The main current is carried by SCR_1, so that load current is flowing through R_L when SCR_1 is fired. If V is large in comparison with the forward voltage drop across SCR_1 when conducting, C will be charged to a voltage V. When SCR_2 is fired, SCR_1 anode will fall to −V. To ensure that SCR_1 remains off, SCR_1 anode must remain reverse biased for a time which is greater than the turn-off time of the SCR (t_{off}). Fig. 2 shows that the voltage across R_L immediately after commutation is 2(V), and the initial current flowing in the load after commutation is $2(V)/R_L$ amps. This current will decay exponentially to zero, that is

$$i = 2(V)\exp(-t/CR_L)/R_L.$$

When V_{RL} has fallen to V, SCR_1 will cease to be reverse biased. That is

$$V_{RL} = iR_L = R_L 2(V)\exp(-t/CR_L)/R_L$$

when

$$V = 2(V)\exp(-t/CR_L)$$

and

$$\exp(-t/CR_L) = 0{\cdot}5.$$

Therefore

$$t/CR_L = 0{\cdot}69.$$

Thus

$$C \geqslant t_{off}/0{\cdot}69R_L\mu F \qquad \ldots(1)$$

where t_{off} is in µs.

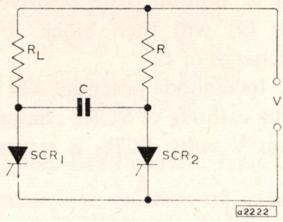


Fig. 1—Bistable circuit

Rate of Rise of Forward Voltage

After commutation, there is a maximum rate at which the forward voltage may be reapplied. For most SCRs this rate is 20 or 25V/µs.

From Fig. 2,

$$V_{SCR} = V - 2(V)\exp(-t/CR_L)$$

and

$$\frac{dv}{dt}_{SCR} = +2(V)\exp(-t/CR_L)/CR_L.$$

Hence, when $t = t_{off}$

$$\frac{dv}{dt}_{SCR} = 2(V)\exp(-0{\cdot}69).0{\cdot}69/t_{off} = 0{\cdot}69(V)/t_{off}. \qquad \ldots(2)$$

A typical value for t_{off} is 20µs, so that V may be as high as 580V before the rate of reapplied voltage exceeds 20V/µs. This figure is in excess of the peak forward voltage of any SCR in the existing Mullard range, so that, in any practical bistable circuit, the rate of voltage change will be within the maximum allowed.

Choice of SCRs

Both SCRs must have the same voltage rating, but generally the switch-off device (SCR_2) may be a lower current type, since its average current is determined by R. However, it must be remembered that during the switch over period, the SCR carries an instantaneous peak current of twice the load current. If the switching rate of the devices is fairly rapid, for example in a d.c. chopping control system, then this peak current will add appreciably to the overall dissipation of SCR_2.

Choice of R when Circuit used with Single Load

Ideally, the higher R is made the better, since a high value of R means little power loss when SCR_2 is conducting. The value of R does, however, determine the maximum switching rate of the system.

If C is to be allowed to charge to full line voltage, then this will take approximately 5CR seconds after SCR_1 has been switched on. Hence this time represents the minimum gating interval between SCR_1 and SCR_2. Since C has been fixed by the load resistance (Eq.1), the maximum value of R can now be determined.

Operation with Inductive Load

The circuit of Fig. 1 can also be used with one inductive load. In this case the value of commutating capacitor could be reduced from that given in Eq.(1). The value required can be obtained from the equation

$$\exp(-\alpha t_{off})\left[2\cos\omega t_{off} - \frac{1}{\omega}\left(\frac{L-2CR_L^2}{LCR_L}\right)\sin\omega t_{off}\right] = 1 \qquad \ldots(3)$$

where

$$\alpha = R_L/2L$$

and

$$\omega = \sqrt{\left(\frac{1}{LC} - \frac{R_L^2}{4L^2}\right)}.$$

Take as an example the case where $t_{off} = 20$µs and $R_L = 10\Omega$.

With a purely resistive load the minimum value of commutating capacitor required is given by Eq.(1) as 2·9µF. If the load has in addition a series inductance of 1mH, the value of the left-hand side of Eq.(3) for different values of C is as given below. For C = 1µF,

$$e^{-0.1}20\cos 0{\cdot}624 - \frac{1}{31\,200}80\,000\sin 0{\cdot}624 = +0{\cdot}10$$

and for C = 2µF,

$$e^{-0.1}2\cos 0{\cdot}436 - \frac{1}{21\,800}30\,000\sin 0{\cdot}436 = +1{\cdot}12$$

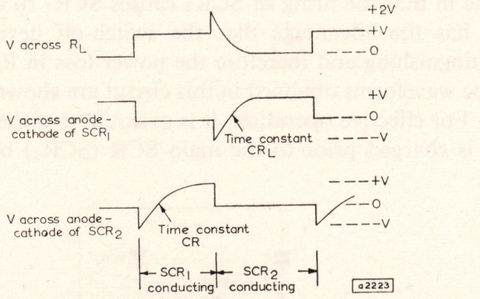


Fig. 2—Waveforms showing time-voltage relationships in bistable circuit

Thus the minimum capacitor required is approximately 1·9µF, compared with 2·9µF for purely resistive loads.

An inductive load will set up a high voltage across SCR_1 after switching. The peak value of this voltage can be calculated approximately by equating energies in the circuit at the moment of switching to energies in the capacitor at the peak of the oscillation. This gives the worst case as in fact the damping action of the resistance of the coil will dissipate energy to the extent of I^2R, where

$$I^2 = \int_{T=0}^{T=\text{time for }V_{max}} i^2 dt$$

and

$$R = \text{resistance of coil.}$$

Thus the approximation is:

$$\tfrac{1}{2}LI_o{}^2 + \tfrac{1}{2}CV_c{}^2 = \tfrac{1}{2}CV_{max}{}^2$$

where

L = inductance of coil in henrys

I_o = current of $\dfrac{\text{supply volts}}{R}$ amps

C = capacitance for commutating in farads

V_c = voltage across capacitor

V_{max} = peak voltage across the capacitor (which, as one plate is at zero volts, will be the peak voltage across the SCR).

If V_{max} is greater than the voltage rating for the SCR, the load must be shunted by a catching diode. The value of commutating capacitance will then be that used with a resistive load of the same resistance as that of the inductance. If two inductive loads are used it is preferable to shunt each of them with a catching diode.

RESONANT CHARGING CIRCUIT

Resonant charging circuits may be used with either resistive or inductive loads. Both methods of operation will be considered.

Circuit Operation with Resistive Load

The circuit shown in Fig. 3 is similar to the previous one in that the firing of SCR_2 causes SCR_1 to extinguish. It has the advantage that the switch-off device is self-extinguishing and therefore the power loss in R is absent. The waveforms obtained in this circuit are shown in Fig. 4.

For effective operation, it is essential that the capacitor C is charged prior to the main SCR (SCR_1) being fired. Thus either SCR_2 must be fired first, or failing this, a high value of resistance R_C is included, and the application of the firing pulse is again delayed after the main line has been switched in.

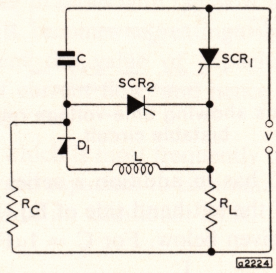


Fig. 3—Resonant charging circuit

The circuit action is as follows:

(i) SCR_1 is fired, causing load current to flow. This also closes the loop C, SCR_1, L and D_1. Now C had previously been charged to V volts (bottom plate negative with respect to top plate). Current will flow round the loop, and assuming the loop losses are small and that V is much greater than the conducting voltage drop across SCR_1 and the diode, this current will continue until C is charged to very nearly V volts in the opposite direction (that is, bottom plate positive with respect to top plate). D_1 will then block, preventing the oscillatory discharge of C.

(ii) SCR_2 is fired. Its cathode potential will rise to $+2(V)$ volts, as will the cathode of SCR_1. Since the anode of SCR_1 is held at V volts, SCR_1 is reverse biased and will extinguish. Then C will discharge through R_L until this current drops below the holding current of SCR_2 when this device will also extinguish.

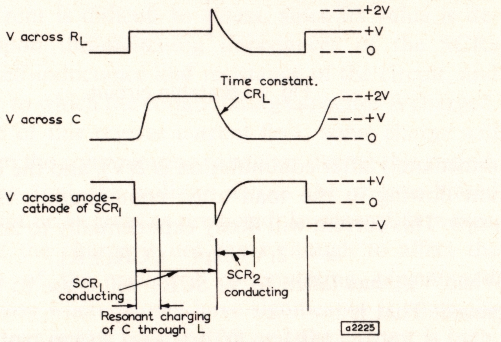


Fig. 4—Waveforms showing time-voltage relationships in resonant charging circuit

Practical Resonant Charging Circuits

If the high resistance R_C is included to give C its initial charge, then a discharge power is also provided after C has charged to 2(V). This imposes a limit on the time for which SCR_1 may be on and then successfully commutated. Even if R_c is omitted, there are still discharge paths provided by the reverse resistance of D_1 and the forward blocking resistance of SCR_2. Hence this circuit cannot maintain its commutating voltage indefinitely.

Circuit Values for Resistive Loads

As in the circuit of Fig. 1, the value of C is defined by the load and the turn off time of SCR_1. That is

$$C \geqslant t_{off}/0{\cdot}69R_L.$$

The value of L must be large enough to reverse bias SCR_2, in a time which is equal to a quarter cycle of oscillation. Hence the minimum value of L is derived from

$$t_{off} = 2\pi\sqrt{(LC)}/4.$$

Therefore

$$L = 4t_{off}{}^2/\pi^2C. \qquad \ldots(4)$$

During the resonant charging of C, the diode must take a peak current whose value is given by

$$i_{peak} = V\sqrt{(C/L)}. \qquad \ldots(5)$$

This peak current requirement determines the choice of diode.

If the diode has a long recovery time, difficulty may be experienced in some circuits. With a diode having a high hole storage charge, after C has charged to its peak value the current will reverse, and will tend to switch off SCR_1 again. This effect is heightened by the sharp cessation of this reverse current in the choke giving rise to an induced voltage.

As in the previous circuit, SCR_2 may be smaller than SCR_1, but it still has to carry a peak current equal to twice the load current. With the minimum values of L and C given above, the maximum operating frequency of the circuit is automatically set. Thus

Minimum period between gating of SCR_1 and SCR_2 = $\sqrt{(LC)}$ sec $\ldots(6)$

Minimum period between gating of SCR_2 and $SCR_1 \simeq 5CR_L$ sec $\ldots(7)$

Circuit Operation with Inductive Load

The inductive load consists of inductance L and resistance R_L and must always be shunted by a catching diode D_1.

For effective operation it is essential that the capacitor C is charged before the main SCR (SCR_1) is fired. The circuit action is as follows:

(i) SCR_2 is fired and thus allows the bottom plate of C to attain zero potential. It then turns off when the current stops flowing through it.

(ii) SCR_1 is fired and thus C is discharged through D_1, L and SCR_1; and, due to the action of L, C is recharged to the reverse polarity so that the bottom plate is at twice the d.c. supply voltage. The diode D_1 then maintains the charge on C, and SCR_1 conducts the load current which rises through $L + R_L$ to its full value V/R_L. Thus the energy in the inductive load L will be $\tfrac{1}{2}LI^2 = \tfrac{1}{2}L(V/R_L)^2$.

(iii) SCR_2 is again fired. The voltage on C appears at the cathode of SCR_1 and thus reverse biases it to the extent of $+V$ volts, so that current ceases to flow in SCR_1. Before SCR_2 was fired, a current of V/R_L was flowing in L. This current attempts to maintain itself because of the energy in L, $\tfrac{1}{2}L(V/R_L)^2$. Thus, when forward current ceases to flow in SCR_1, the load current must be drawn from the capacitor C. If the energy $\tfrac{1}{2}CV^2$ in C is small compared with the energy $\tfrac{1}{2}LI^2$ in L then C may be considered to discharge linearly. SCR_1 ceases to be reverse-biased when there is zero voltage across C.
Thus for linear discharge $Q = CV$ and $Q = It$, therefore $t = CV/I$,
where
t = time for C to discharge = reverse bias time for SCR_1 (at least 25μs is recommended)
V = d.c. supply voltage
I = V/R_L of full load current for SCR_1.
The capacitor C, after discharge, recharges until the bottom plate reaches zero potential. At this point the diode D_1 accepts negative current and thus dissipates the remaining inductive energy in the load.

(iv) SCR_1 is again fired and the cycle of (ii) and (iii) repeated.

If the diode D_1 has a long recovery time it is likely that SCR_1 will be turned off before it starts to conduct load current. One method of overcoming this difficulty is to keep the gate of SCR_1 energised throughout its conducting period. However, making L as large as practicable will also help.

Precise Phase Angle Control of SCRs

R. A. Payne

Mullard Semiconductor Measurement and Application Laboratory

This article describes a circuit which will provide an output to an SCR gate variable from zero to10ms, giving control of the conduction angle from 0 to 180°. The design procedure is explained, and the results obtained from a practical circuit are given.

INTRODUCTION

SCR firing circuits for applications such as the control of lighting and electric furnaces, in which the load is mainly resistive, are well known, and pulse firing methods are normally employed. When the load is highly inductive, however, as is the case with field regulators for large alternators, it is much better to maintain the SCR gate energised throughout the conducting half-cycle.

The circuit described here has been designed for this purpose, and at the same time to switch on the SCR in a variable relation to the 50c/s sinewave and allow it to switch off at the zero point of the wave. The variation is controlled by a positive d.c. signal voltage, which thus provides phase control.

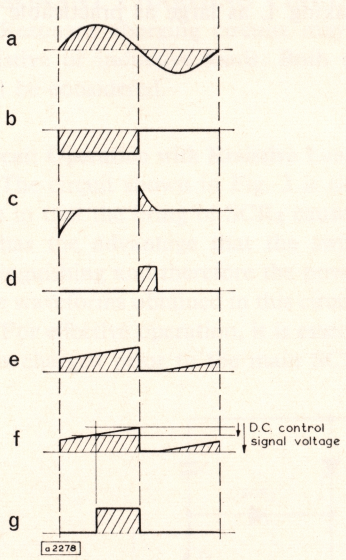


Fig. 1—Production of firing pulse from sinewave input

The first requirement of the equipment is that the zero point of the 50c/s wave be determined. The wave (Fig. 1a) is fed to a pulse amplifier which gives a square wave output (Fig. 1b). This is differentiated to short positive and negative pulses (Fig. 1c) which are synchronous with the zero points of the sinewave. The pulses which occur when the sinewave is going negative (Fig. 1d) are then used to reset the sawtooth shown in Fig. 1(e), while the d.c. control voltage determines how much of the sawtooth (Fig. 1f) is passed to the output amplifier. Finally (Fig. 1g) the output amplifier produces a pulse of the same duration as its input, but of a form suitable for the particular gate drive required.

CIRCUIT

The layout of the circuit is shown in the block diagram of Fig. 2 and the circuit diagram, Fig. 3. This circuit provides an output that is temperature-stable to approximately one degree reduction in conduction angle for 5degC increase in temperature, up to 60°C ambient. A 20% change of a.c. supply voltage produces less than one degree change in firing angle. Control is provided by a positive d.c. voltage of from 1 to 4V.

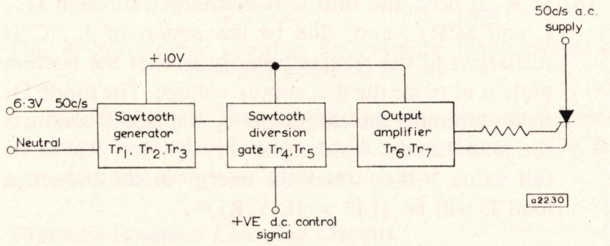

50c/s a.c. supply
+10V
6·3V 50c/s
Neutral
Sawtooth generator Tr1, Tr2, Tr3
Sawtooth diversion gate Tr4, Tr5
Output amplifier Tr6, Tr7
+VE d.c. control signal
a2230

Fig. 2—Schematic diagram of equipment

The block diagram, Fig. 2, shows the main sections of the circuit, which are:

(i) Sawtooth generator synchronised to the main supply frequency

(ii) Sawtooth diversion gate controlled by the input signal voltage

(iii) Output amplifier.

Sawtooth Generator

The capacitor C$_2$ is discharged via Tr$_3$ once every cycle by a 2ms pulse which is derived from the 6·3V r.m.s. sinusoidal input from the mains supply. The pulse is formed by using the negative half sinewave to bias Tr$_1$ into the off state, this transistor being normally on. The resulting fast edges at the collector are then differentiated, and the positive pulse amplified by Tr$_2$ to give the 2ms pulse duration required at the base of Tr$_3$.

Sawtooth Diversion Gate

Transistor Tr$_4$ remains non-conducting until the sawtooth voltage applied to its emitter becomes more positive than the voltage at its base. The charging current for C$_2$ (Fig. 3) is then diverted to the base of Tr$_6$, the output amplifier.

The voltage applied to the base of Tr$_4$ is controlled by Tr$_5$ which is in turn controlled by the input signal voltage. Tr$_5$ converts the input voltage from positive with respect to earth, to negative with respect to the +10 V supply.

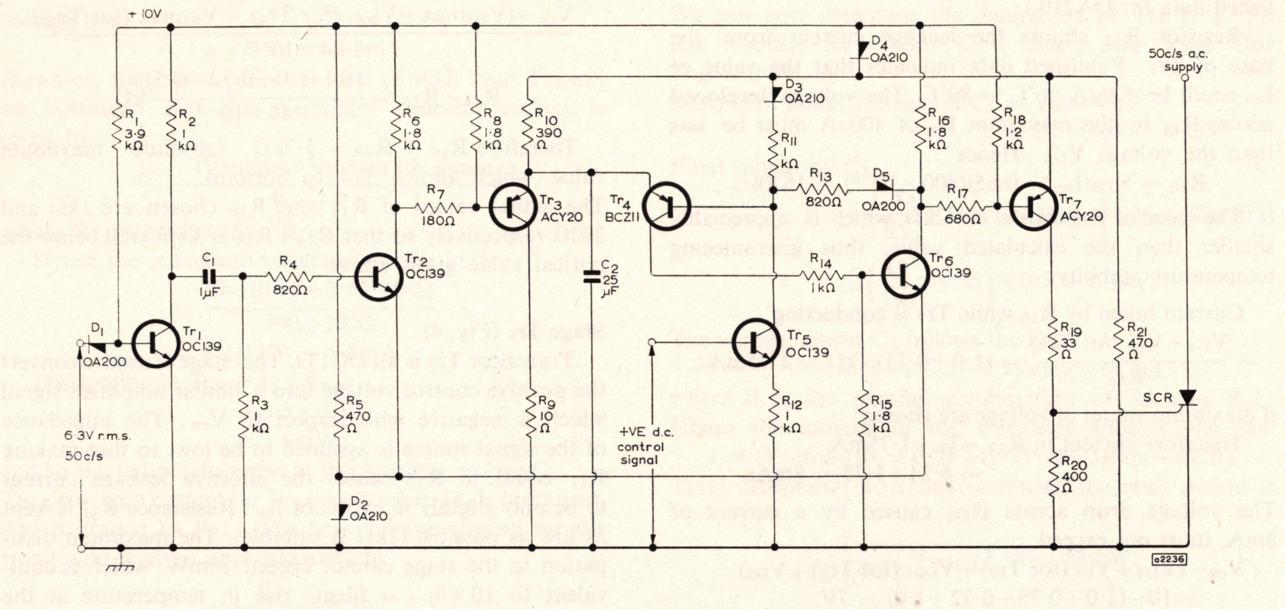

+10V
R1 3·9 kΩ
R2 1 kΩ
R6 1·8 kΩ
R8 1·8 kΩ
R10 390 Ω
D4 OA210
D3 OA210
50c/s a.c. supply
R11 1 kΩ
R16 1·8 kΩ
R18 1·2 kΩ
R7 180Ω
Tr3 ACY20
Tr4 BCZ11
R13 820Ω
D5 OA200
R17 680Ω
Tr7 ACY20
C1 1μF
R4 820Ω
Tr2 OC139
C2 25 μF
R14 1kΩ
Tr6 OC139
D1 OA200
Tr1 OC139
Tr5 OC139
R19 33 Ω
R21 470 Ω
R3 1 kΩ
R5 470 Ω
R9 10 Ω
+VE d.c. control signal
R12 1 kΩ
R15 1·8 kΩ
SCR
6·3V r.m.s. 50c/s
D2 OA210
R20 400 Ω
a2236

Fig. 3—Conduction angle control circuit

Output Amplifier

The output amplifier consists of two transistors Tr$_6$ and Tr$_7$ and provides an output of 9V across an equivalent load of 33Ω to the SCR gate. This output is sufficient to fire the full range of Mullard SCRs.

Power Supply Requirements

All tests on the circuit were carried out with V$_{cc}$ as a stabilised positive d.c. supply of 10V, and taking not more than 500mA current.

The operation of the circuit is synchronized to the mains supply by the pulse shaper which is driven by 6·3V r.m.s. (peak current 2mA) derived from the mains.

DESIGN PROCEDURE

Stage Tr$_7$ (Fig. 4)

A previous article showed that an output of 9V across an equivalent load of 33Ω is suitable. The d.c. supply voltage, V$_{cc}$, is +10V, and Tr$_7$ is an ACY20.

From the figures given (assuming that the input impedance of the SCR when fired is very small) the collector current of Tr$_7$ is

$$I_c = \frac{(V_{ce} - \text{voltage across } D_4)}{R_{19}} = \frac{(10-0{\cdot}65)}{33} = 282\text{mA}.$$

If we assume 10 per cent tolerance in R$_{19}$ we get a top limit of collector current of 282×1·1 = 310mA. If the bottom limit value of current gain of the ACY20 is 50, the top limit of base current required by Tr$_7$ is given by

$$I_B = 310/50 = 6{\cdot}2\text{mA}.$$

The maximum collector dissipation of Tr$_7$ is given by the product of the maximum collector current and the top limit of bottomed potential.

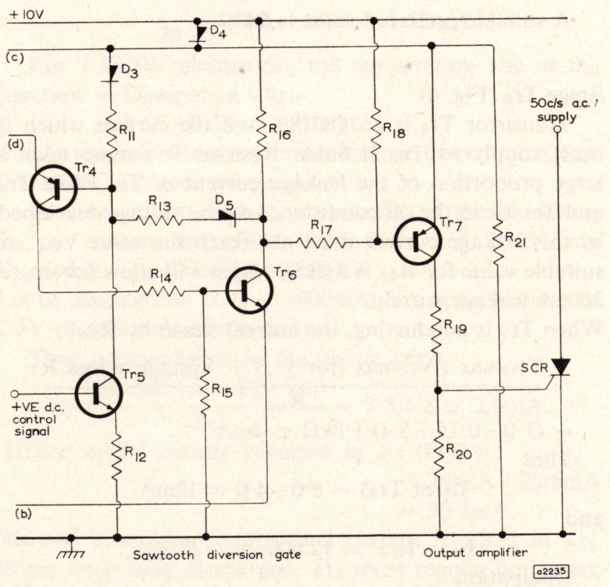

+10V
(c)
D4
D3
50c/s a.c. supply
R11
R16
R18
(d)
Tr4
R13
D5
R17
Tr7
R21
R14
Tr6
R19
Tr5
R15
SCR
+VE d.c. control signal
R12
R20
(b)
Sawtooth diversion gate
Output amplifier
a2235

Fig. 4—Sawtooth diversion gate and output amplifier

Hence

$$W_c\text{max} = I_c\text{max} \times V_{\text{bott}}\text{max} = 310 \times 0{\cdot}5 = 155\text{mW}.$$

When the control is such that the SCR conducts over half a cycle (the conduction angle is 180°), the drive transistor Tr$_7$ dissipates the above energy for only half of each 20ms period. Thus the mean dissipation to be expected in Tr$_7$ under worst conditions is 78mW. The transistor Tr$_7$ is not mounted on a heatsink, and the thermal resistance (junction to case) is 0·25deg C/W, so that the expected temperature rise above ambient under worst conditions is $78 \times 0{\cdot}25 = 19{\cdot}5$degC, and so for a 60°C ambient the junction temperature can reach nearly 80°C.

The emitter of Tr_7 is biased negative by the voltage across the diode D_4, which is maintained at not less than 0·65V by feeding it with approximately 20mA maintaining current via the 470Ω resistor R_{21}. (See published data for OA210.)

Resistor R_{18} shunts the leakage current from the base of Tr_7. Published data indicates that the value of I_{co} could be 400μA at $T_j = 80°C$. The voltage developed across R_{18} by the maximum I_{co} of 400μA must be less than the voltage V_{D4}. Hence

$$R_{18} = V_{D4}/I_{co} = 0{\cdot}65/(400 \times 10^{-6}) = 1620\Omega.$$

The value of R_{18} chosen is 1·2kΩ, which is appreciably smaller than the calculated value, thus guaranteeing temperature stability.

Current taken by R_{18} while Tr_7 is conducting

$$= \frac{V_{D4} + V_{be}\text{ (for }Tr_7)}{R_{18}} = (1{\cdot}0 + 0{\cdot}75)/1\text{k}\Omega = 1{\cdot}75\text{mA},$$

if maximum values of voltage are chosen.

Therefore current in $R_{17} = I_B + 1{\cdot}75$mA

$$= 6{\cdot}24 + 1{\cdot}75 = 8\text{mA}.$$

The voltage drop across R_{17}, caused by a current of 8mA, must not exceed

$$V_{cc} - (V_{D4} + V_{be}\text{ (for }Tr_7) + V_{bott}\text{ (for }Tr_6) + V_{D2})$$
$$= 10 - (1{\cdot}0 + 0{\cdot}75 + 0{\cdot}22 + 1{\cdot}0) = 7\text{V}.$$

Hence

$$R_{17} = 7{\cdot}0/(8 \times 10^{-3}) = 875\Omega.$$

A suitable preferred value is 680Ω.

Stage Tr_6 (Fig. 4)

Transistor Tr_6 is an OC139, and the current which it must supply to Tr_7 is 8mA. Resistor R_{16} must take a large proportion of the leakage current of Tr_6 while Tr_6 and Tr_7 are in the off condition, and the voltage developed by this leakage current must not reach the value V_{D4}. A suitable value for R_{16} is 1·8kΩ, which will allow for up to 360μA leakage current.

When Tr_7 is conducting, the current taken by R_{16}

$$= \frac{V_{D4}\text{max} + V_{be}\text{max (for }Tr_7) + \text{Voltage across }R_7}{R_{16}}$$
$$= (1{\cdot}0 + 0{\cdot}75 + 5{\cdot}4)/1{\cdot}8\text{k}\Omega \simeq 4\text{mA}.$$

Thus

$$I_c\text{(for }Tr_6) = 8{\cdot}0 + 4{\cdot}0 = 12\text{mA}$$

and

$$I_B = I_c/\alpha' = 12\,000/20 = 600\mu\text{A}.$$

Dissipation

$$= I_c \times V_{bott} = 12 \times 0{\cdot}5 = 6\text{mW},$$

and so the average dissipation (½ cycle) = 3mW.

Temperature rise of junction = Dissipation × θ_{j-c}, and $\theta_{j-c} = 0{\cdot}5$degC/W.

Therefore

$$T_j \text{ for 60°C ambient} = 61{\cdot}5°\text{C}.$$

From published data, $I_{co} = 100\mu$A at 61·5°C.

Resistor R_{15} is used to shunt the leakage of Tr_6 from its base. It also carries the collector leakage current for Tr_4 (I_{co} for Tr_4 is less than 10μA). The value of R_{15} is taken as 1·8kΩ.

During conduction, the current in R_{15}

$$= \frac{V_{D2}\text{max} + V_{be}\text{max (for }Tr_6)}{R_{15}} = \frac{1{\cdot}0 + 0{\cdot}5}{1{\cdot}8\text{k}\Omega} = 0{\cdot}84\text{mA}.$$

Now

$$I_b = 0{\cdot}6\text{mA},$$

hence current required in $R_{14} = 1{\cdot}44$mA.

Thus $R_{14} + R_{10}$ should not exceed

$$\frac{V_{cc} - (V_{D2}\text{max} + V_{bott}\text{ (for }Tr_4) + V_{be}\text{max (for }Tr_6))}{1{\cdot}44 \times 10^{-3}}$$
$$R_{14} + R_{10} = \frac{10 - (1{\cdot}0 + 0{\cdot}32 + 0{\cdot}5)}{1{\cdot}44 \times 10^{-3}}\text{k}\Omega.$$

Therefore $R_{14} + R_{10} = 5{\cdot}7$kΩ (absolute maximum value which allows Tr_7 to bottom).

The actual values of R_{14} and R_{10} chosen are 1kΩ and 390Ω respectively so that $R_{14} + R_{10}$ is kept well below the critical value given above.

Stage Tr_5 (Fig. 4)

Transistor Tr_5 is an OC139. This stage is used to convert the positive control voltage into a similar amplified signal which is negative with respect to V_{cc}. The impedance of the signal source is assumed to be low, so that making R_{11} equal to R_{12} causes the effective leakage current to be only slightly in excess of I_{co}. Resistance R_{11} is kept as low as possible (1kΩ is suitable). The maximum dissipation in the stage cannot exceed 10mW, which is equivalent to $10 \times \theta_{j-c} = 5$degC rise in temperature at the junction.

Thus

$$T_j\text{max} < 65°\text{C for 60°C ambient}$$

and

$$I_{co} < 125\mu\text{A}.$$

We can now determine the change of voltage at the collector of Tr_5 caused by a change in leakage current.

Room Temp.	25°C	60°C
T_j	30°C	65°C
I_{co}	12μA	120μA

From 25°C to 60°C the maximum change of $I_{co} = 108\mu$A.

The change of voltage at the collector of Tr_5 = change of $I_{co} \times R_{11} = 108$mV.

This would introduce an error in phase shift at the output.

The voltage gain of the stage is unity, as $R_{11} = R_{12}$, and $I_c = V_{IN}/R_{12}$ (V_{IN} = Signal voltage).

However, for an input of 4V, $I_c = 4/1000 = 4$mA.

Therefore

$$I_B\text{max} = I_c/\alpha'\text{min} = 4000/20 = 200\mu\text{A}.$$

The input impedance to the control stage will be approximately $\alpha' R_{12}$, which gives a variation of between 20×10^3 and $80 \times 10^3\Omega$, or from 20kΩ to 80kΩ input impedance according to the value of α′ for an OC139.

Stage Tr_4 (Fig. 4)

Transistor Tr_4 is a type BCZ11. This stage controls the point on the sawtooth ramp at which the capacitor charging current is diverted to the base of Tr_6.

Transistor Tr_4 conducts when its emitter becomes more positive than the voltage at the collector of Tr_5.

To bottom Tr_7, I_b (for Tr_6) must be not less than 1·44mA.

Thus the minimum drive voltage (with respect to the h.t. line) is $I_c \times R_{10}$

$$= \frac{1{\cdot}44}{10^3} \times 390 = 560\text{mV}.$$

This minimum value is exceeded by V_{D3} under normal conditions.

The maximum current in R_{10} = maximum drive voltage/R_{10}

$$\simeq 4/390 \simeq 10{\cdot}3\text{mA}.$$

However, there is a collector load of 1kΩ. Thus Tr_4 will be bottomed and the maximum collector current is given by

$$\frac{V_{cc} - (V_{D2}\text{min} + V_{D3}\text{min} + V_{D4}\text{min})}{R_{10} + R_{14}}$$

where R_{14} is greater than R_{10}.

Hence the maximum collector current in Tr_4

$$= \frac{10 - (0{\cdot}65 + 0{\cdot}65 + 0{\cdot}6)}{390 + 1000}$$
$$= 8{\cdot}1/1390 = 5{\cdot}8\text{mA}.$$

Dissipation in $Tr_4 = I_c \times V_{bott}$

$$= 5{\cdot}8 \times 0{\cdot}32$$
$$\simeq 1{\cdot}9\text{mW},$$

and so the temperature rise at the junction ≃ 1degC.

The peak base current for Tr_4 occurs when Tr_4 is bottomed, and is limited by R_{12}. The base voltage applied for the worst case is given approximately by

$$\frac{R_{11}}{R_{12} + R_{11}} \times V_{cc}$$
$$\simeq 7{\cdot}5\text{V}.$$

Therefore

$$I_B\text{max} \simeq 7{\cdot}5/R_{11} = 7{\cdot}5/1000 = 7{\cdot}5\text{mA}.$$

Stage Tr_3 (Fig. 5)

Transistor Tr_3 is an ACY20. By experiment, a suitable value for C_2 is 25μF (tantalum). This may be reduced to 10μF without serious adverse effects, but further reduction tends to produce oscillation at about 1kc/s at the Tr_7 output.

The time-constant chosen for the sawtooth-forming circuit is 10ms, which gives an acceptably linear voltage ramp over a period of 18ms (20ms minus the 2ms allowed for reset).

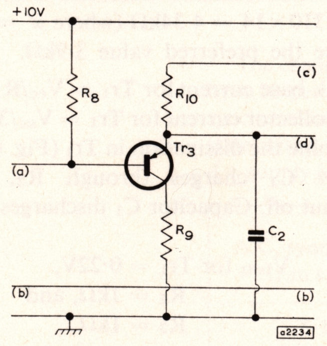


Fig. 5—Sawtooth Generator

Now

$$V_{cc} = 10\text{V and } I_{c(pk)}\text{max for ACY20} = 1\text{A}$$

Hence, to limit the peak current, 10Ω is used as a collector load. This gives a discharge time-constant of 25μF × 10Ω = 250μs. To allow full discharge of the capacitor a discharge time of five times this time-constant is allowed, that is 5 × 250 = 1·25ms.

(Preferred component values give a 2ms pulse.)

To provide 1000mA collector current

$$I_b = I_c/\alpha' = 1000/35 = 28{\cdot}6\text{mA}.$$

(α'_{min} reduces to 35 at high currents.)

We can now determine the dissipation in Tr_3 (Fig. 5). $R_{10} = 390\Omega$; $R_9 = 10\Omega$; $C_2 = 25\mu$F; and V_{bott} (for Tr_3) = 0·5V.

Maximum initial voltage on $C_2 = V_{cc} - V_{D3}$

$$= 10 - 0{\cdot}65 = 9{\cdot}35\text{V}.$$

Final voltage on C_2

$$= \left(\frac{R_9}{R_{10}} \times \text{Initial voltage}\right) + V_{bott}\text{ (for }Tr_3)$$
$$= \left(\frac{10}{390} \times 9{\cdot}35\right) + 0{\cdot}5 = 0{\cdot}74\text{V}.$$

The voltage across C_2 follows the law

$$V = 0{\cdot}73 + (9{\cdot}35 - 0{\cdot}73)\exp(-t/CR)$$

where R is the parallel combination of R_9 and R_{10}.

Hence the current in the transistor follows the law

$$I = (V - 0{\cdot}5)/10 = 0{\cdot}23 + (9{\cdot}35 - 0{\cdot}73)\exp(-t/CR)$$

Total dissipation in transistor during the reset period is

$$\frac{1}{2 \times 10^{-3}} \int_0^{2 \times 10^{-3}} V_{bott} \times I\,.\,dt = 68\text{mW}.$$

Thus the average dissipation over 20ms is

$$\frac{2}{20-2} \times 68 = 68/9 = 7{\cdot}55\text{mW}.$$

For 7·55mW dissipation, the temperature rise at the junction = Dissipation × θ_{j-c}

$$= 7{\cdot}55 \times 0{\cdot}25 = 1{\cdot}82\text{degC}.$$

This is equivalent to a maximum leakage current of 100μA for a 60°C ambient temperature.

Because of the high peak current in the transistor, R_8 is chosen as 1·8kΩ, and from published data V_{be} (when $I_c = 300$mA) = 750mV.

Let us assume that at $I_c = 1000$mA, V_{be} approximates to 2·5V (it will certainly be less).

Then current taken by R_8 (worst case)

$$= \frac{V_{D3}\text{max} + V_{be}\text{ (for }Tr_3)}{R_8} = 3{\cdot}5/1{\cdot}8 \simeq 2{\cdot}0\text{mA}.$$

Hence initial current required in R_7 (Fig. 3)

$$= 2{\cdot}0\text{mA} + 28{\cdot}6\text{mA}$$
$$= 30{\cdot}6\text{mA}.$$

We can now calculate the final current required in R_7. When C_2 is fully discharged, Tr_3 must remain bottomed, and therefore

$$I_c = \frac{V_{cc} - V_{D3}\text{min}}{R_{10} + R_9} = \frac{10 - 0{\cdot}65}{390 + 10} = \frac{9{\cdot}35}{400} \simeq 23\text{mA}.$$

Thus

$$I_B = I_c/\alpha' = 23000/50 = 460\mu\text{A}.$$

From published data, the maximum base current of the ACY20 is 50mA. Hence R_7 must not be less than

$$\frac{V_{cc} - (V_{D2}\text{min} + V_{D3}\text{min})}{I_{B(pk)}\text{max}} = \frac{10 - (0{\cdot}65 + 0{\cdot}65)}{50 \times 10^{-3}}$$
$$= \frac{8{\cdot}7}{50} \times 10^3 = 174\Omega.$$

We adopt the preferred value, 180Ω.

Thus the voltage drop in R_7 when C_2 is fully discharged

$$= R_7 \times I_{\text{Bfinal}}$$
$$= 180 \times 460 \times 10^{-6}$$
$$= 83\text{mV}.$$

Stage Tr_2 (Fig. 6)

Transistor Tr_2 is an OC139. Since the current taken by R_8 = 2·0mA, it will be seen that the initial current in R_7 = 30·6mA. Thus the initial voltage drop in $R_7 = (30{\cdot}6 \times 180)/10^3 = 5{\cdot}5\text{V}$.

The voltage drop between the base of Tr_3 and the positive supply $= V_{D3}\text{max} + V_{be}\text{max}$ (for Tr_3)

$$= 3{\cdot}5\text{V}.$$

Thus the initial voltage drop across $R_6 = 5{\cdot}5 + 3{\cdot}5$

$$= 9{\cdot}0\text{V}.$$

Hence the initial current in $R_6 = 9/1800 = 5{\cdot}0\text{mA}$, and the total drive current required at the collector of Tr_2,

$$I_c = 5{\cdot}0\text{mA} + 30{\cdot}6\text{mA} = 35{\cdot}6\text{mA}.$$

Therefore

$$I_B = I_c/\alpha' = 35{\cdot}6/18 \simeq 2\text{mA},$$

(where $\alpha' = 18$ is derived from the published data). The collector current for Tr_2 will not exceed

$$V_{cc}/R_6 + V_{cc}/R_7$$
$$= 10/1800 + 10/180 \simeq 60\text{mA}.$$

Hence the maximum dissipation will be less than $60 \times V_{\text{bott}}$ (where $V_{\text{bott}} = 0{\cdot}22$)

$$= 13{\cdot}2\text{mW for 2ms}.$$

Thus the average dissipation $\simeq 13{\cdot}2/9 = 1{\cdot}47\text{mW}$.

Stage Tr_1 (Fig. 6)

Transistor Tr_1 is an OC139, and the input voltage, $V_{IN} = 6{\cdot}3\text{Vr.m.s.}$

(The value of V_{IN} is limited by the maximum allowable reverse V_{be} for Tr_1). Resistor R_1 is used to just bottom Tr_1, assuming that the load consists of R_2, R_4, and R_3, all in parallel.

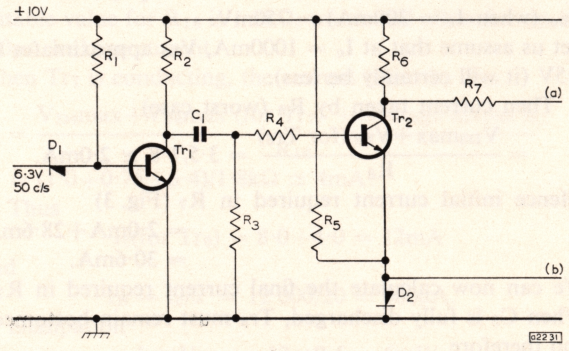


Fig. 6—Input stage

Voltage V_{IN} is applied to D_1, which conducts negative current only and shuts off Tr_1 as the supply turns negative; D_1 protects Tr_1 against forward current from the supply. Transistor Tr_1 again conducts as V_{IN} becomes more positive, and thus a positive pulse is transmitted to Tr_2 via C_1. The duration of this pulse is determined by the time-constant which is given by

$$C_1 \times [R_2 + R_4R_3/(R_4+R_3)].$$

The leakage current for Tr_2 passes through R_4 and R_3. The maximum leakage current for Tr_2 with an ambient temperature of 60°C could be 100μA, and the voltage drop caused by the current of 100μA in R_4+R_3 should not exceed 0·65V. Thus the value of R_4+R_3 should not exceed $0{\cdot}65\Omega/(100 \times 10^{-6})$

$$= 6{\cdot}5\text{k}\Omega.$$

To provide a suitable time-constant in the differentiating network referred to below, values of

$$R_3 = 1\text{k}\Omega$$
$$\text{and } R_4 = 820\Omega \text{ were chosen.}$$

The drive current required for the base of Tr_2 = 2mA.

Hence the voltage across R_4 when Tr_2 conducts

$$= 2\text{mA} \times 820$$
$$= 1{\cdot}64\text{V}.$$

Thus the voltage across $R_3 = 1{\cdot}64 + V_{D2}$

$$= 2{\cdot}44\text{V}.$$

Resistor R_2 must take the leakage current for Tr_1 and provide a suitable component for the differentiating network. Its value is set at 1kΩ. The time-constant should be at least 1·25ms.

A suitable value for C_1 is 1μF; this gives a time-constant of 1·45ms.

We can now determine the duration of the pulse. The voltage applied to R_3 is of the form $10\exp(-t/RC)$, and this reaches 2·44V when

$$t = -RC\log_e(2{\cdot}44/10).$$

Inserting the values for R and C, we find t = 2ms, so that the pulse duration is 2ms.

Resistor R_2 must allow sufficient base current to bottom Tr_1 with a collector load equivalent to R_2, R_3 and R_4 all in parallel. If we call this R_e, we have

$$R_e = \frac{R_3R_4}{R_3+R_4} \times R_2 \Bigg/ \frac{R_3R_4}{R_2+R_3+R_4}.$$

Now

$$I_c = V_{cc}/R_e \text{ and } I_B = V_{cc}/R_1 = I_c/\alpha'$$

whence

$$R_1/\alpha' = R_e = R_2R_3R_4/(R_3R_4 + R_2R_3 + R_4R_2)$$

hence

$$R_1/\alpha' = 450 \times 1000/1450 = 310\Omega.$$

Thus

$$R_1 = 310 \times 14 = 4{\cdot}34\text{k}\Omega \text{ (where } \alpha' = 14)$$

and we choose the preferred value 3·9kΩ.

Hence the peak base current for $Tr_1 = V_{cc}/R_1 = 2{\cdot}56\text{mA}$, and the peak collector current for $Tr_1 = V_{cc}/310 = 32\text{mA}$. We can determine the dissipation in Tr_1 (Fig. 6) as follows. The capacitor C_1 charges through R_2, R_3 and R_4 when Tr_1 is shut off. Capacitor C_1 discharges through Tr_1 and R_3, and

$$V_{\text{bott}} \text{ for } Tr_1 = 0{\cdot}22\text{V},$$
$$R_2 = 1\text{k}\Omega, \text{ and}$$
$$R_3 = 1\text{k}\Omega.$$

The current through Tr_1 is given by

$$I = (V_{cc} - V_{\text{bott}})/R_2 + (V_{cc} - V_{\text{bott}})\exp(-t/CR)/R_3$$

Therefore the dissipation in Tr_1 for the conducting half-cycle is

$$0{\cdot}22(9{\cdot}78/10^3) + 0{\cdot}22\int_{0}^{10\times10^{-3}} 10^{-3} \times 9{\cdot}78\exp(-t/CR).$$

$$\simeq 2{\cdot}15\text{mW}.$$

Thus the average dissipation in $Tr_1 \simeq 1{\cdot}08\text{mW}$.

The point at which the positive-going pulse is applied to Tr_2 is determined by the point at which current starts to flow in D_1. This occurs at a point V_{D1}, and the delay due to this voltage drop can be calculated using $u = V\sin\omega t$. It should be noted that V_{be} for Tr_1 should be added to V_{D1}. Both values change with temperature, but the temperature effect is small and has not been allowed for.

Now

$$u = V\sin\omega t,$$

and so

$$u/V = \sin\omega t.$$

Thus

$$\omega t = \sin^{-1}(u/V)$$

and so the delay

$$t = \sin^{-1}(u/V)/\omega$$

Taking typical values,

$$\omega = 2\pi f,$$
$$f = 50\text{c/s},$$
$$u = V_{D1} + V_{be} \text{ (for } Tr_1),$$
$$V_{D1} = 0{\cdot}6\text{V},$$
$$V_{be} \text{ (for } Tr_1) = 0{\cdot}3\text{V},$$

and

$$V = 6{\cdot}3\sqrt{2} = 8{\cdot}9\text{V}.$$

Thus

$$t = \sin^{-1}(0{\cdot}9/8{\cdot}9)/2\pi 50$$
$$= 0{\cdot}00319\sin^{-1}0{\cdot}101.$$

Hence the delay = 322μs, and is very nearly constant over the design temperature range.

APPENDIX

EXPERIMENTAL RESULTS

TABLE I

The d.c. supply for V_{cc} remained constant at +10V. The a.c. supply for synchronising remained constant at 6·3Vr.m.s. The a.c. supply frequency remained constant at 50c/s.

Conduction period (ms)	Control signal voltage (V)				
Ambient Temperature	20°C	30°C	40°C	50°C	60°C
Zero	1·62	1·62	1·58	1·56	1·54
1	1·76	1·74	1·73	1·70	1·68
2	1·92	1·90	1·88	1·86	1·85
3	2·08	2·07	2·06	2·04	2·02
4	2·27	2·26	2·24	2·23	2·22
5	2·48	2·46	2·45	2·44	2·44
6	2·70	2·69	2·67	2·67	2·67
7	2·95	2·94	2·93	2·93	2·93
8	3·24	3·22	3·22	3·22	3·22
9	3·56	3·54	3·54	3·54	3·55
10	3·87	3·88	3·88	3·90	3·90

TABLE II

The temperature remained constant at 25°C. The a.c. synchronising supply remained constant at 6·3Vr.m.s. The a.c. supply frequency remained constant at 50c/s.

Conduction period (ms)	Control voltage (V)		
D.C. supply for V_{cc} (V)	8·5	10·0	12·0
Zero	1·38	1·62	2·00
1	1·49	1·76	2·20
2	1·61	1·91	2·40
3	1·75	2·08	2·65
4	1·90	2·27	2·90
5	2·07	2·47	3·18
6	2·26	2·70	3·46
7	2·46	2·95	3·80
8	2·72	3·23	4·12
9	3·00	3·55	4·54
10	3·30	3·87	5·00

TABLE III

The change in the duration of the conduction period caused by a 20 per cent change in the nominal voltage of the a.c. synchronising supply was seen to be almost constant at any set state within the operating conditions of the circuit, with the d.c. supply for V_{cc} set at +10V.

A.C. synchronising supply r.m.s. voltage (V)	Change in conduction period (μs)
6·3+20%	+40
6·3−20%	−30

TABLE IV

The d.c. supply voltage for V_{cc} remained constant at +10V the a.c. supply for synchronising remained constant at 6·3Vr.m.s. The a.c. supply frequency remained constant at 50c/s.

Conduction period (ms)	Control voltage (V)	Control voltage (V)	Current taken from d.c. supply for V_{cc} (mA)		Current taken from positive d.c. control signal (μA)	
Temperature	25°C	60°C	25°C	60°C	25°C	60°C
Zero	1·62	1·54	88	90	45	27
1	1·76	1·68	102	104	49	32
2	1·92	1·85	115	117	53	35
3	2·08	2·02	129	130	58	39
4	2·27	2·22	142	142	64	44
5	2·48	2·44	155	156	70	50
6	2·70	2·67	168	170	76	56
7	2·95	2·93	182	182	84	63
8	3·24	3·22	194	196	92	72
9	3·56	3·55	207	208	102	81
10	3·87	3·90	220	220	112	92

With the equipment used, the accumulated experimental error in the readings given in Tables I to IV should not exceed 5 per cent.